Design and Development of Thyristor based MLCR CSC

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ABSTRACT

The new concept of **Multi-Level Current Reinjection (MLCR)** combines the advantages of DC ripple reinjection, multi-level conversion and soft-switching technique. Taking advantage of the soft-switching technique which uses zero current switching for the main bridge switches, thyristor based MLCR current source converter (CSC) is proposed. This concept adds self-commutation capability to thyristors and produces high quality line current waveforms. Various thyristor based MLCR CSC topologies have been simulated extensively using PSCAD/EMTDC in this thesis and their performance characteristics investigated.

Questions have been raised about the ability to force the main thyristors off using the reinjection bridge in a real-world implementation, where there are inevitable stray capacitances and inductances which may influence the thyristor turn-off; and simulation switching models may not represent the switching characteristics fully or accurately. For this proof of concept, a small-scale prototype has been built in the laboratory. The 3-level MLCR CSC, which increases the pulse number from 12 to 24, is chosen to verify the concept. The experimental investigation of the 3-level MLCR CSC, under steady-state conditions, verified the following:

- The reinjection current allows the main bridge thyristors to be switched at negative firing angles.
- This current reinjection technique allows self-commutation capability in a practical system despite the finite turn-off times of the thyristor.
- This current reinjection technique improves the harmonic characteristics of the thyristor based converter.
- It is observed that the deviation of the actual waveforms from the theoretical waveforms is mainly due to the snubber across the reinjection switch, and a trade-off in the choice of snubber components is required.

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GLOSSARY

NOMENCLATURE

AC	Alternating Current
BTB	Back-To-Back
CSC	Current Source Converter
DC	Direct Current
ESEDS	Error Square Error Derivative Square
FACTS	Flexible AC Transmission System
GTO	Gate Turn Off Thyristor
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
LC	Line Commutated
LCL	Inductor Capacitor Inductor
MLCR	Multi-Level Current Reinjection
MLCR CSC	Multi-Level Current Reinjection Current Source Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
p.u.	per unit
PCB	Printed Circuit Board
PI	Proportion and Integration
PWM	Pulse Width Modulation
PWM-VSC	Pulse Width Modulation Voltage Source Converter
RCD	Resistor Capacitor Diode

RMS	Root Mean Square
SCR	Short Circuit Ratio
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
ZCD	Zero Crossing Detector
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

ABBREVIATIONS

α	Firing angle
β_i	Reinjection IGBT switching angle
$\frac{n_i}{n_0}$	Turns ratio of reinjection transformer
μ	Commutation angle
C	DC blocking capacitor
C_{dc}	DC-side capacitance
C_{sn}	Snubber capacitance
E_{dc}	DC-side load voltage
F	Form factor
f_s	Switching frequency
f_{reinj}	Reinjection Transformer operating frequency
f_{source}	Source frequency
f_{sY}/f_{sD}	Voltage Switching function for α = -45°
$gy1$	Trigger pulse for thyristor Y1
H_{Li}	Step height of an m-level linear reinjection waveform
H_{Si}	Step height of an m-level ESEDS reinjection waveform
$I_a/I_b/I_c$	AC-side line current
I_1	DC bus current connected to Y-Y bridge
I_2	DC bus current connected to Y-D bridge

I_{a1}	Peak value of fundamental component of line current I_a
I_{aD}	Y-D connected AC-side line current
I_{arms}	RMS value of line current I_a
I_{aY}	Y-Y connected AC-side line current
$I_{aY}rms$	RMS rating of line current I_{aY}
I_{caD}	Y-D connected AC-side phase current
I_{dc}	Output DC current
I_g	Gate drive current
I_{inj}	Reinjected current to main bridge
I_{j1}	Reinjection transformer primary-side current connected to Y-Y bridge
I_{j2}	Reinjection transformer primary-side current connected to Y-D bridge
I_{si}	Reinjection current through reinjection bridge IGBT
I_{thyY1}	Current flowing through thyristor Y1 in Y-Y bridge
I_Trms	RMS rating of current through main bridge thyristor
k_n	Turns ratio of main transformer
$L_a/L_b/L_c$	AC-side source inductance
L_{dc}	DC-side smoothing inductance
P_{dc}	Output DC power
R_{dc}	DC-side load resistance
R_g	Gate drive resistor
R_{sn}	Snubber resistor
S_{pi}/S_{ni}	Reinjection bridge IGBT switching pair
T_a	Ambient temperature
$V_a/V_b/V_c$	AC-side source voltage
$V_d\ (dc)$	DC voltage across DC blocking capacitor connected to Y-D bridge
$V_y\ (dc)$	DC voltage across DC blocking capacitor connected to Y-Y bridge
$V_{control}$	Analog firing angle control
V_{dc}	Output DC voltage
V_d	DC-side voltage across Y-D bridge

$V_d\ (ac)$	Reinjection transformer primary-side voltage connected to Y-D bridge
V_m	Reinjection transformer secondary-side voltage
V_{pk}	AC-side line-to-ground peak voltage
V_{ramp}	Ramp voltage produced by TCA 785
V_{ripple}	Voltage ripple across DC blocking capacitor
V_{sensed}	Input AC sensed voltage
V_x	DC-side voltage across 12-pulse bridge
V_y	DC-side voltage across Y-Y bridge
$V_y\ (ac)$	Reinjection transformer primary-side voltage connected to Y-Y bridge
V_z	Voltage across reinjection IGBT switching pair
X_c	DC blocking capacitor impedance
$Y-D$	Star-Delta connected bridge
$Y-Y$	Star-Star connected bridge

Chapter 1

INTRODUCTION

1.1 GENERAL OVERVIEW

High Voltage Direct Current (HVDC) transmission systems are being used increasingly in the present context today. The first commercial HVDC system was the 20 MW/100 kV Gotland-1 link which was commissioned in 1954, using Mercury-arc converters valves. There was a significant improvement in HVDC technology in the 1970s when thyristor valves were introduced in place of the mercury arc valves. The power rating of the Gotland 1 rating increased to 30 MW/150 kV in 1970. For the first time in the world, thyristor valves were used in a commercial HVDC transmission. Subsequently, with the increase in thyristor voltage and current ratings, the power rating of HVDC transmission systems increased. Transmission voltages of ±600 kV to ± 800 kV are classified as ultraHVDC (UHVDC). There are a number of ongoing UHVDC projects in China, India and North America, the largest being the Jinping/Sunan HVDC (± 800 kV/7200 MW) in China. The A5000 thyristor valve [Kunpeng *et al.* 2012], made up of 8.5 kV/5 kA 6-inch thyristor is used in the Jinping/Sunan HVDC converter. Today, there are 151 thyristor based HVDC projects world-wide (either in operation or planned for the very near future) [IEEE/PES 2011].

The advantages of HVDC transmission systems as compared to High Voltage AC (HVAC) transmission system are well known. Long distances are technically not feasible by HVAC lines without intermediate reactive power compensation [Meah and Ula 2007] - [Sousa *et al.* 2012]. The per unit cost of a HVDC line is lower than that of a HVAC line when the transmitted power rating increases. For example, the first 6000 MW stage of the transmission for the Three Gorges Project in China would have required 5×500 kV AC lines as opposed to $2 \times \pm 500$ kV HVDC lines as shown in Fig. 1.1 [Canelhas 2010].

Recently, the focus on large offshore wind-farms has increased and many studies are being carried out to determine the best transmission system between the offshore wind-farm and the shore. HVDC transmission is preferable to HVAC transmission for distances above 70 kilo-meters [Negra *et al.* 2006]. Using extensive simulation, it was shown that using the HVDC link, offshore and

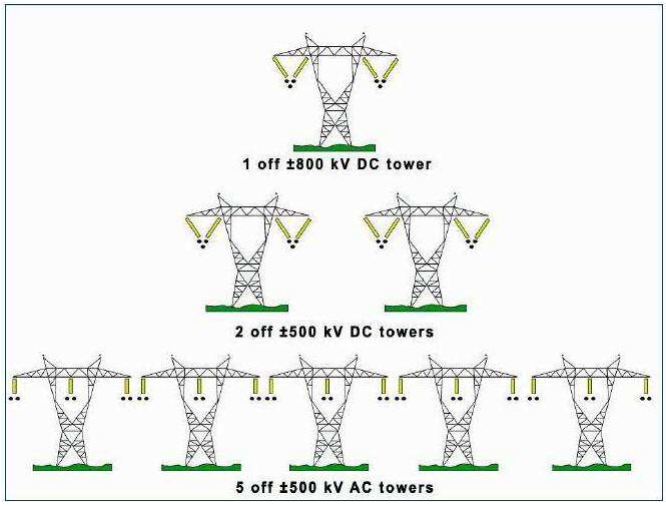


Figure 1.1: Transmission footprint comparison between HVDC and HVAC.

onshore grids would not affect each other during grid faults [Chou *et al.* 2012]. Also, for a fault in the offshore grid, the voltage and frequency response in the onshore grid is more stable under the HVDC link than those under the HVAC link or HVAC link combined with STATCOM. A similar economic comparison of capital costs and losses for extraHVAC (EHVAC) and DC transmission alternatives for a hypothetical 1200 kilo-meters, 3000 MW transmission system was presented in [Bahrman 2008], which showed that HVDC is very attractive when compared to EHVAC. Hence, thyristor based HVDC systems are a key solution in future transmission systems.

On the other hand, recent advances in power semiconductor devices (IGBT/IGCT with maximum ratings available today of around 6.5 kV/6 kA) have allowed self-commutated converters to become an intrinsic component in medium voltage HVDC systems. These are referred to as voltage source converter (VSC) HVDC systems using pulse width modulation converter (PWM). PWM-VSC is marketed as:

- **HVDC-Light** by ABB, commissioned first in Sweden (*Hällsjön* HVDC, ±10 kV, 3 MW), in 1997. Power electronic interface comprises of a PWM-VSC based on IGBTs.
- **HVDC-Plus** by Siemens commissioned first in the USA (Transbay Cable HVDC,±200 kV, 400 MW), in 2010. Power electronic interface comprises of multi-level VSC based on IGBTs.

As VSCs utilize self-commutating switches, it can produce its own sinusoidal voltage waveform using pulse-width modulation (PWM) independent of the AC network voltage, removing some of the issues of the thyristor based current source converters (CSC) such as reactive power support, commutation failure, line current harmonics, etc.

With a multi-level PWM-VSC, the harmonic content of the voltage produced by the VSC is so

low that minimal or no filtering equipment is necessary; whereas for two-level and three-level converters, additional filters are required. Irrespective of which topology is used, PWM-VSC can always be treated as an ideal AC voltage source where the controller specifies the magnitude, phase and frequency of the produced sinusoidal voltage waveform. A brief comparison with thyristor based HVDC reveals that PWM-VSC HVDC:

- does not require any commutating voltage source for commutation. As the converter works independently of any voltage source, it is less sensitive to disturbances in the network.
- reduces the chances of commutation failure.
- provides independent control of active and reactive power without any need for extra compensating equipment.
- allows the control systems on both sides to operate independently of each other.
- has multi-level configurations drastically reducing the filtering requirements.
- has the ability to supply passive loads.

All existing self-commutating HVDC systems to date utilise PWM-VSCs. Since their introduction in 1997, PWM-VSC HVDC installations have steadily increased in power ratings thanks to incremental developments in cable system, control system and the IGBT switch ratings. There are now PWM-VSC links around the world operating in the 400 MW range at ±200 kV (Transbay link and BorWin 1). Several HVDC Plus projects with 690 MW/±320 kV are under construction (Borwin 2, Helwin1, 2, SylWin1).

Further to this, DolWin 2, the 900 MW PWM-VSC HVDC (ABBs HVDC Light ±320 kV) is currently under construction for commissioning in 2015. In 2011 the development of the Skagerrak 4 interconnection link was announced. This will be a 500 kV/700 MW monopole system due for commissioning in 2014. This implies that the capability exists today for a 1400 MW VSC HVDC system. Presently, the Skagerrak 4 HVDC Light link will be operated in a bipole configuration with the Skagerrak 3 Thyristor CSC HVDC link.

The two or three-level PWM based schemes are designed for use at high frequencies. This causes high dv/dt at the switching instants. Thus additional snubber circuits are required which result in additional losses. Minimal on-state and switching losses require relatively low switching frequencies which are on the high side when PWM is used. A comparison, provided by ABB [Persson 2011] for the power loss of the complete converter showed that:

- An IGBT based Generation 1 HVDC Light has a power loss $\approx 3\%$ with switching frequency close to 2 kHz.

- An IGBT based Generation 4 HVDC Light has a power loss $\approx 1\%$ with switching frequency down to 1 kHz.
- A thyristor based line-commutated (LC) converter including switches, filters, and transformers has a power loss of 0.8%.

While assessing the energy loss in a converter, one of the most important factor is the switching frequency used. An efficiency comparative study is carried out in [Wiechmann *et al.* 2008] where one of the scenarios include high power 20 MW application. The losses of the PWM-VSC are nearly 50% higher than those of the thyristor based CSC topology.

Currently, all of the installed HVDC Light systems are either back-to-back (BTB) converters or are connected through underground cables. No overhead DC lines have been installed as of yet. When a line-to-ground fault occurs on the DC-side, the IGBTs lose control and free-wheeling diodes conduct and feed the fault. In overhead lines, faults may occur due to storms or when lightning strikes the line. This may cause the line to break, fall to the ground and create a fault. Ground faults may also occur by objects such as trees, falling onto the line and providing a path to ground. By keeping the DC cable underground these situations are avoided. However, underground faults can still occur when insulation of the cable fails due to improper installation, excessive voltage/current, environmental factors or ageing. Similarly, line-to-line faults on underground systems are less likely to occur because of line insulation and earth separation. Because of the inherent topology of HVDC Light systems, they are defenceless against DC faults and AC protection must isolate the fault.

UHVDC transmission is only justified for the transmission of very large power over very long distances. This calls for the use of overhead transmission lines. Thyristor based HVDC with long overhead transmission lines are naturally able to withstand short circuit currents due the DC inductors limiting the current during fault conditions and the ability of thyristors to isolate the fault path. For long distances, underground cables will have huge laying costs and reliability issues, as cable length will be limited and there would be many joints. As such, the use of HVDC Light for UHVDC will not be considered in the near future till topology and protection issues related with using overhead cables are addressed. Underground DC superconductor cables are presented as a new alternative for high power long distance transmission of electric power [McCall *et al.* 2010] which will rival traditional HVDC cables and overhead HVAC lines.

A possible alternative to two or three level conversion for high voltage application is the multi-level concept. Many multi-level concepts have been proposed [Arrillaga *et al.* 2009]:

- Diode clamped VSC.
- Flying capacitor clamped VSC.

- Cascaded H-bridge VSC.
- Modular Multi-level Converter.

To meet harmonic standards, these multi-level converters need to have high level numbers which increase the converter complexity. The diode clamped topology needs a large number of clamping diodes while capacitor clamped topology needs high capacity clamping capacitors. Capacitor voltage balancing requires a complicated control strategy. The complexities in topological structures and other associated problems have limited the level number of these converters to a low value. Out of these, only the Modular Multilevel Converter (MMC) has been used by the industry as HVDC-Plus. MMC [Lesnicar and Marquardt 2003] is a new and promising technology for HVDC. The topology was introduced in 2003 and the development towards a commercial technology has been very fast. MMC converters have several features such as high modularity, high power quality and low loss operation that make them suitable for HVDC [Friedrich 2010], [Li and Zhao 2010]. MMC is suited for overhead transmission because of the adequate protection it offers for DC faults. The losses are lower because the switching frequency is 50 Hz. However, the main challenge is the complex topology and its control and the need to maintain the floating capacitor at the reference value. The present HVDC Plus technology uses IGBTs and there is no reason why it should not use IGCTs instead, which will reduce the switching losses further.

CSCs based on PWM schemes are reported in [Rodrguez *et al.* 2005]. These converters are termed as PWM-CSC. Significant accomplishments have been achieved for PWM-CSC, such as harmonic distortion minimization [Hombu *et al.* 1987], high-input power factor [Xiao *et al.* 1998], reduced switching frequencies [Espinoza *et al.* 1995], etc. However, there are very few proposals on PWM-CSC for HVDC/FATCS applications [Yamada *et al.* 1990], [Ye *et al.* 2005], [Stretch *et al.* 2006], [Torres Olguin *et al.* 2013]. The main reasons behind the choice of PWM-VSC over PWM-CSC so far and why PWM-CSC can be considered for future projects are as follows:

1. The CSCs require switches that are capable of blocking voltages of both polarities. IGBTs with anti-parallel diodes are therefore not appropriate for CSCs. A series diode needs to be added, increasing cost and losses. Again, as mentioned earlier, IGCTs solve this problem. The IGCT is optimized for low conduction losses. Its typical turn-on/off switching frequency is in the range of 500 Hz. However, the switching frequency can be increased up to 40 kHz, where it is limited by the operating thermal losses and cooling system design.

2. The DC-side in a CSC requires an inductor, whereas in PWM-VSC it requires a capacitor. The power loss of an inductor is expected to be larger than that of a capacitor. Thus, the efficiency of a PWM-CSC is expected to be lower than that of a VSC. However, HVDC system is intended to transmit power over long distances. The DC line inductance will be significant for a long line. This line inductance may make up a large portion of the

required inductance at the DC-side for free! Also, the DC-side losses can be minimized using super-conductive materials in the construction of the DC-side reactor.

3. In PWM-VSC, reactive power and DC current/voltage can be controlled independently. This means that reactive power requirements can be eliminated. However, reactive power control is simpler in PWM-CSC as the current in the AC-side is directly controlled.

Although PWM-CSC can offer good performance, in PWM-CSC the forced commutation from rated current to zero involves large electromagnetic energy being dissipated in the AC system inductances. The interfacing of the PWM-CSC with an AC system requires expensive capacitors to provide a path for transfer of the current. This has been the main problem of PWM-CSC. Additionally, PWM-CSC based schemes are designed for use at high frequencies which will result in higher switching losses.

Another issue is that the AC-side filter capacitors resonate with the AC-side inductances. As a result, some of the harmonic components present in the output current might be amplified, causing high harmonic distortion in the AC-side current. The problem of the resonance between the capacitances and inductances on the AC-side can be mitigated by carefully designing the filter capacitor and introducing sufficient damping using proper control methods.

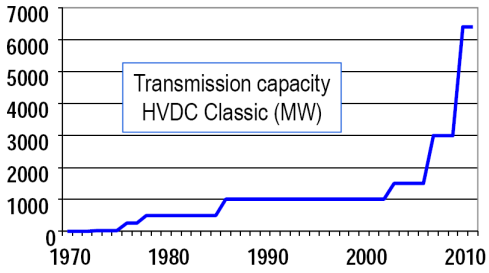
Considering the above merits and demerits, an effective large power conversion system should have the following characteristics:

1. High quality current waveforms.
2. Low dv/dt across switches.
3. Minimal on-state and switching loss thereby requiring low switching frequency.
4. Simple structural topology to reduce costs.
5. Independent active and reactive power control.

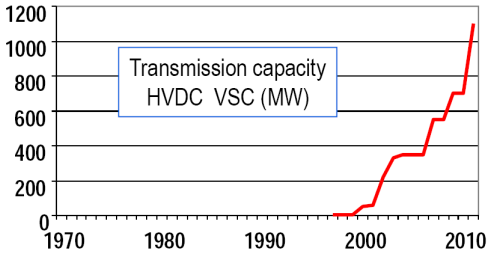
It is now established that PWM-VSC technology is well suited to medium voltage levels but will not be able to catch up with the thyristor based HVDC in terms of power handling capacity in the very near future (Fig. 1.2). Hence, *there is a clear incentive for research in the thyristor based HVDC technology.* The research on thyristor based HVDC is focused on:

- achieving force commutation with thyristors;
- operating with negative firing angles enabling reactive power export;
- operating under the thyristors under zero current switching which would even lower the losses, voltage stress and costs;

- reducing the harmonic distortion caused by thyristor based converters.



(a): Thyristor based HVDC.



(b): PWM-VSC HVDC.

Figure 1.2: Transmission capacity comparison between Thyristor HVDC and PWM-VSC HVDC.

1.1.1 Soft-Switching for HVDC

The concept of soft-switching reduces the switching losses by forcing the current in and/or voltage across a power switch to be close to zero, at the beginning of and during the switching process, thereby reducing the turn-on di/dt and the turn-off dv/dt the switching device is subjected to. Inductive snubbers and two auxiliary switches are used to achieve zero-current commutations in the main switches [Tomasin 1995]. Another topology which achieves zero voltage switching (ZVS) or near zero current switching (ZCS) with an LCL resonant circuit at the output was proposed in [Dieckerhoff *et al.* 1999].

A self-commutated PWM-CSC HVDC system with soft-switching technique is proposed in [Senjyu *et al.* 1999]. Switching losses with 120° operation have been calculated, and an improvement in power loss of more than 50% of total losses for hard-switching PWM-VSC is obtained. However, the LC commutation circuit which achieves the ZCS condition is connected in the main power transfer path, which is a drawback.

The main features of the soft switching technique for high power applications should be:

1. the main bridge switch ratings should not be increased due to the circulation of energy used by the soft switching network.

2. the soft switching network should be only activated by control signals synchronised with the main bridge control signals such that ZCS conditions occur at the appropriate instant.

The concept of multi-level current reinjection (MLCR), proposed in [Perera 2006] presents a different form of soft switching technique. ZCS condition is achieved through forced clamping using reinjection switches [Arrillaga *et al.* 2006]. ZCS condition is achieved before the main bridge switching occurs and finishes after the main bridge switching is over. The reinjection switches

are synchronised with the firing control of the main bridge which ensures that controllable ZCS durations are obtained. This ZCS scheme is totally different from the LC resonant soft-switching scheme. With controllable ZCS (achieved by controlling the width and height of the multilevel reinjection steps using the reinjection bridge), self-commutation is added to a thyristor converter. Based on this concept, various thyristor based MLCR CSC schemes have been proposed:

- A STATCOM where the MLCR CSC operates as a statcom under symmetrical and asymmetrical line voltages achieving fast dynamic response to system changes [Liu *et al.* 2006].
- A back-to-back (BTB) HVDC link where BTB MLCR HVDC with parallel connected 12-pulse bridge converter operates satisfactorily with varying active and reactive power operating conditions [Liu *et al.* 2007a].
- A standard HVDC link where MLCR HVDC scheme with the standard 12-pulse bridge converter operates with the same waveform quality and control flexibility of PWM-VSC schemes [Liu *et al.* 2007b].
- A superconducting magnetic energy storage (SMES) where series connected paralleled MLCR CSCs are used to achieve four quadrant control [Murray *et al.* 2009].

1.2 THESIS OBJECTIVE

Thyristor based HVDC system is still the key for future high power transmission. The MLCR concept combines the advantages of reinjection, soft-switching and multi-level conversion, and it does not utilize PWM. This is an exciting alternative to the present HVDC schemes.

However, questions have been raised about the ability to force the main thyristors off using the reinjection bridge in a real-world implementation, where there are inevitable stray capacitances and inductances which may influence the thyristor turn-off; and simulation switching models may not represent the switching characteristics fully or accurately. The objective of this thesis is to design and develop a small-scale prototype thyristor based MLCR CSC for conclusive proof of the MLCR concept.

To be able to achieve this objective, various PSCAD/EMTDC simulation models were developed which were used to carry out an initial evaluation study for a 3-level, 5-level and 7-level thyristor based MLCR CSC in terms of line current total harmonic distortion (THD) obtained, reinjection transformer requirements, reinjection switch ratings, and reinjection control circuitry complexities. Based on these results, the 3-level MLCR CSC which increases the pulse number from 12 to 24, was implemented in the laboratory to verify whether neglecting some of the real-world artifacts will impede the operation of a practical MLCR CSC or not.

1.3 THESIS CONTRIBUTION

The work in this thesis has lead to the design and development of the first experimental prototype of the MLCR CSC concept. This has led to these significant results:

- **Achieving self-commutation with thyristors**- the design and development of the small-scale prototype experimentally demonstrated the ability to force turn-off the thyristors in the main bridge of the 12-pulse converter by using added reinjection switches.
- **Ability to operate thyristors with negative firing angles**- the successful operation of the prototype proved that the main bridge thyristors can commutate without the assistance of the line-commutating voltage. This is done by modifying the DC bus currents of the 12-pulse converter and designing zero current duration in such a way that they are sufficient enough to permit the off-going thyristor to re-establish its voltage blocking ability. Reactive power control is now possible.
- **Reduction in AC-side line current THD**- the modification of the DC bus current into a varying DC waveform lowers the AC-side line current harmonic distortion caused by thyristor based MLCR CSC. This allows thyristors, (rather than self-commutation devices like IGBT/IGCT) to be used in the main bridge.
- **Reduction in switching loss**- the ability to use thyristors in the main bridge leads to an increase in the efficiency of the converter as thyristors have lower switching losses when compared to other self-commutating devices. A comparison between LC CSC, PWM-VSC and MLCR CSC is presented for this purpose.

1.4 THESIS OUTLINE

This thesis contains 8 chapters.

Chapter 2 briefly presents a comprehensive review of power quality improvements made by applying the concept of DC ripple reinjection in current source series connected AC-DC rectifier using PSCAD/EMTDC. The limitations of the original DC ripple reinjection concept are also presented.

Chapter 3 discusses the fundamentals of the multi-level reinjection concept for a 12-pulse CSC which includes the ideal reinjection waveform and two approximations proposed: the ESEDS and linear reinjection waveforms. The synthesis of reinjection waveforms for hardware implementation is also briefly discussed.

Chapter 4 uses the ZCS achieved by linear reinjection waveform to describe the thyristor based MLCR-CSC. A comparative evaluation study is carried out for a 3-level, 5-level and 7-level thyristor based MLCR CSC in terms of line current THD obtained, reinjection transformer requirements, reinjection switch ratings, and reinjection control circuitry complexities. This chapter also includes the selection of the DC blocking capacitor and the choice of snubber components for the 3-level MLCR CSC.

Chapter 5 describes the hardware implementation of the 12-pulse thyristor based converter: its hardware modules and experimental results. Hardware details for extension of the firing pulses to have a firing angle range of $-180^\circ \leq \alpha \leq 180^\circ$ using TCA 785 phase controller is presented along with a new forward converter based thyristor gate driver circuit. The implementation details of an opto-coupler based IGBT driver circuit for the reinjection switches are presented. This chapter also describes the hardware modules used to generate the reinjection pulses for a 3-level MLCR CSC. A section on reinjection transformer testing is also included.

Chapter 6 provides the experimental results for the 3-level MLCR CSC. The ability of the main bridge thyristors to switch at negative firing angle is verified. The trade-off in the choice of the snubber circuit is illustrated with its influence on the AC-side current and DC-side voltage of the 3-level MLCR CSC.

Chapter 7 provides a comparative study for making an initial trade-off assessment in the choice of an HVDC converter among LC CSC, PWM-VSC and the 7-level MLCR CSC based on New Zealand Pole 2 ratings.

Chapter 8 discusses the general conclusions, and the scope for future work in the area of thyristor based MLCR CSC is identified.

Chapter 2

BACKGROUND

2.1 INTRODUCTION

The non-linear operation of thyristor based AC-DC converter causes highly distorted line currents resulting in distorted line voltage. This distortion is one type of the power quality problem. Power quality is actually a misnomer. While it is a convenient term, it is actually the quality of the voltage or current waveforms.

To effectively deal with this problem, various techniques both on AC as well as DC-side of the converter have been proposed so far. Usually, filters (which may be passive, active or hybrid) are used depending upon rating and economic considerations. Multi-pulse converter is another simple and effective method for reducing line current harmonics. These converters involve multiple rectifiers so connected that the harmonics produced by one is cancelled by the other. Multi-pulse converters such as 12, 18, 24 and 36-pulse rectifiers are used nowadays and the THD of the input line current is reduced to 15.2%, 10.1%, 7.5% and 5.3% respectively [Syafri *et al.* 2002], [Choi *et al.* 1996], [Karnath *et al.* 2002], [Singh *et al.* 2007]. Multi-pulse rectifiers are usually fed by complex phase shifting transformers. Different phase shifting transformers include T-connected, Zigzag, Fork, Delta and Double star, Polygon, Inter-Phase, etc. The THD of the line current is getting reduced with increasing pulse number, but the THD reduction is getting smaller and smaller from 18-pulse to 30-pulse configuration while the complexity of the phase shifting transformer increases. While these transformers are useful for low-voltage applications, these have been found to be uneconomical in the HVDC system [Arrillaga *et al.* 2007]. An extensive review on the multi-pulse AC-DC converters is presented in [Singh *et al.* 2008].

The use of harmonic injection as a method of harmonic reduction in 6-pulse converters was first proposed by [Bird *et al.* 1969]. This concept introduced the idea of using the third harmonic injection to modify the rectifier current waveform in order to reduce the AC-side current harmonic content. This concept was further investigated in [Ametani 1972]. He injected other harmonics such as 5^{th}, 7^{th}, 9^{th} etc. and concluded that the third harmonic is the most suitable for these, while the ninth harmonic is the most appropriate for the reduction of harmonics higher than the

ninth. The main disadvantages of the harmonic injection concept were:

- the need of an external third-harmonic current generator and its synchronization with the source.
- the inability to modify more than one harmonic order at any operating condition.
- the difficulty in adjusting the amplitude and phase of the injected harmonic current for different operating condition.

These practical difficulties led a halt in the research in this area till around 1980. In 1980, DC ripple reinjection concept was introduced in [Baird and Arrillaga 1980] - [Arrillaga *et al.* 1983] to increase pulse number of line-commutated 6-pulse AC-DC converter. This method reduces line current harmonics both on the AC and DC-side. Over the years the original DC ripple reinjection scheme has been subjected to many changes to achieve pulse multiplication using several reinjection transformers and a corresponding increase in the number of reinjection switches. The main aim of this chapter is to present a review of the DC ripple reinjection concept over the years.

2.2 DC RIPPLE REINJECTION

2.2.1 6-pulse converter without DC ripple reinjection

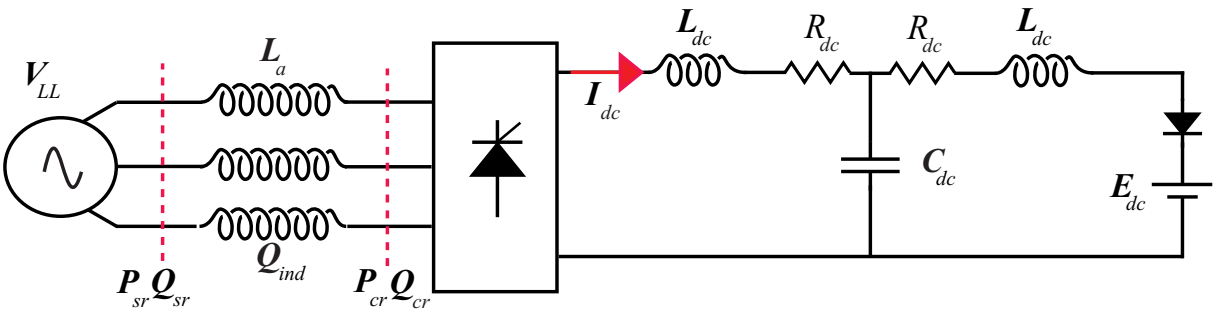


Figure 2.1: Simplified simulated 6-pulse converter.

The basic module of the thyristor based AC-DC converter is the Graetz Bridge, the basic 6 pulse current source converter (CSC). The Graetz Bridge is universally used for HVDC converters as it provides best switch and transformer utilization factor [Padiyar 1990].

The CIGRE benchmark model for HVDC is the standard model implemented in PSCAD or MATLAB for HVDC studies [Faruque *et al.* 2006]. A simplified closed loop 6-pulse converter is shown in Fig. 2.1, without any AC filter, is simulated using PSCAD/EMTDC with the parameters listed in Table 2.1.

Table 2.1: Simulated System Parameters for 6-pulse Converter.

Simulation parameters	Actual values
AC source voltage ($V_{an}/V_{bn}/V_{cn}$)	232 kV
Source Inductance ($L_a/L_b/L_c$)	42.7 mH
DC voltage (V_{dc})	500 kV
DC current (I_{dc})	2 kA
DC-side inductor (L_{dc})	0.5968 H
DC-side resistance (R_{dc})	2.5 Ω
DC-side capacitance (C_{dc})	26 μF
DC voltage at inverter (E_{dc})	490 kV

Table 2.2 shows the active and reactive power requirements for the 6-pulse converter. It can be clearly inferred that the majority of reactive power generated by the source is consumed by the converter (almost 70%). The reason for this is the use of firing angle control. The thyristors do not start to conduct at the natural firing instant (i.e when voltage across it becomes positive). Instead, the thyristors are fired after a delay equal to the firing angle (α). Also, as the thyristor is fired, the current does not commutate instantaneously from the outgoing thyristor to the incoming thyristor. This delay is the commutation angle (μ) and is due to energy transfer between phase inductances, and would be higher for a system with higher line inductances. Thus line currents always lag the phase voltage, and the converter will consume reactive power, which is almost 40% of the total active power. The reactive power consumed by the converter is supplied from the AC-side. It can be understood that this converter is capable of transferring active power only and has no control on the reactive power. An independent control of active and reactive power is not possible.

Table 2.2: Active and Reactive Power values without DC Ripple Reinjection.

Simulated parameter	Value
Source active power, P_{sr}	1000 MW
Source reactive power, Q_{sr}	428 MVAR
Converter active power, P_{cr}	1000 MW
Converter reactive power, Q_{cr}	312 MVAR
DC power, P_{dc}	1000 MW

Another major disadvantage is the large amounts of harmonic voltages and currents generated both on the AC and DC-side respectively. An ideal 6-pulse rectifier generates characteristic current harmonics of the order: $h = 6k \pm 1$ on the AC-side and voltage harmonics of the order: $6k$ on the DC-side, where k = 1, 2, 3,... etc. The AC-side line current THD obtained is 25.1%.

2.2.2 6-pulse converter with DC ripple reinjection

The basic DC ripple reinjection applied to the simplified 6-pulse converter (Section 2.2.1) is shown in Fig. 2.2 where the DC ripple of the 6-pulse voltage, V_{out}, is used as the commutating voltage for the harmonic injector (single-phase thyristor controlled bridge in this case) which injects a current component on the AC-side producing a 12-pulse waveform. The reinjection circuit consists of two single-phase transformers connected across the bridge through two DC blocking capacitors (C). The two reverse-connected secondary windings are in series with the DC bus via the harmonic injector. Capacitors (C) block the DC component of V_a and V_b producing $V_{a_{ac}}$ and $V_{b_{ac}}$.

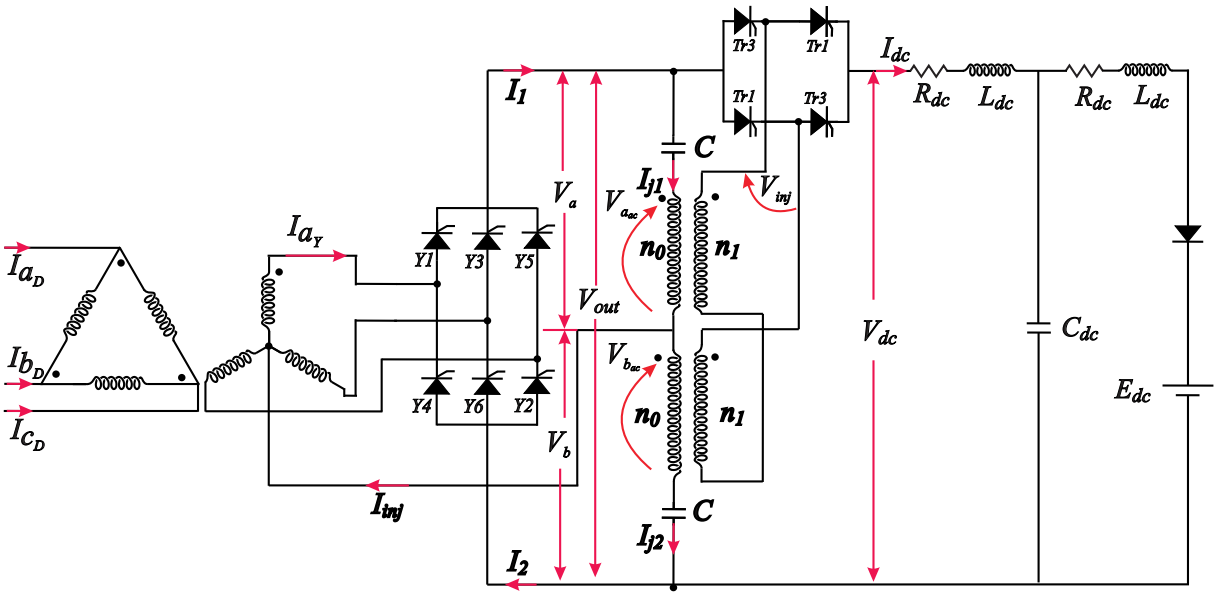


Figure 2.2: 6-pulse converter with DC ripple reinjection.

The injected voltage is:

$$V_{inj} = \frac{n_1}{n_0} \cdot (V_{a_{ac}} - V_{b_{ac}}) = \frac{n_1}{n_0} \cdot (V_a - V_b) \tag{2.1}$$

This voltage acts as the commutating voltage for the harmonic injector and also gets added to output DC voltage V_{dc}. The reinjection thyristors T_{r1} and T_{r3} are fired 30° after the corresponding main bridge thyristors as shown in Fig. 2.3.

The turns ratio for the reinjection transformer is [Baird and Arrillaga 1980]:

$$\frac{n_1}{n_0} = \frac{1}{2}\left[1 - tan^2\left(\frac{\pi}{24}\right)\right] = 0.464 \tag{2.2}$$

Assuming I_{dc} is smooth, the injection current I_{inj} is composed of the following: When T_{r1} conducts: $I_{j1} = \frac{n_1}{n_0} I_{dc}$ and when T_{r3} conducts: $I_{j1} = -\frac{n_1}{n_0} I_{dc}$. Current I_{inj}, with frequency

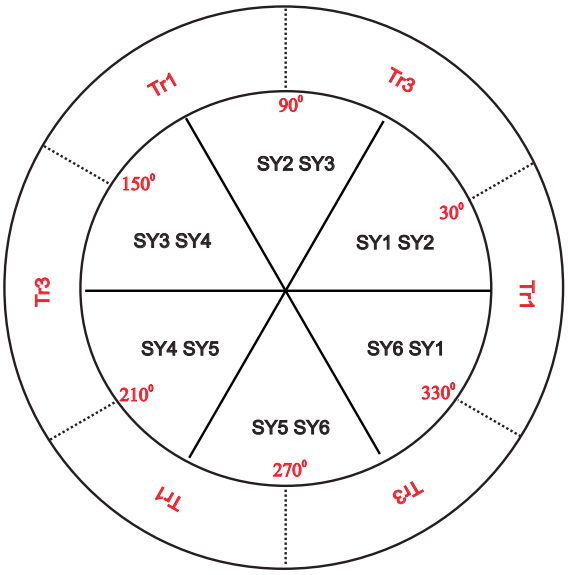


Figure 2.3: Firing sequence of 6-pulse converter with DC ripple reinjection.

three times the fundamental, is injected into the mid-point of the Y-connected secondary-side of interface transformer. I_{inj} modifies the both the secondary and primary-side line currents, and the overall current THD for I_{aD} is reduced to 14.3%. The secondary and primary-side line currents are shown in Fig. 2.4. V_{dc}, I_{dc} and I_{inj} are shown in Fig. 2.5.

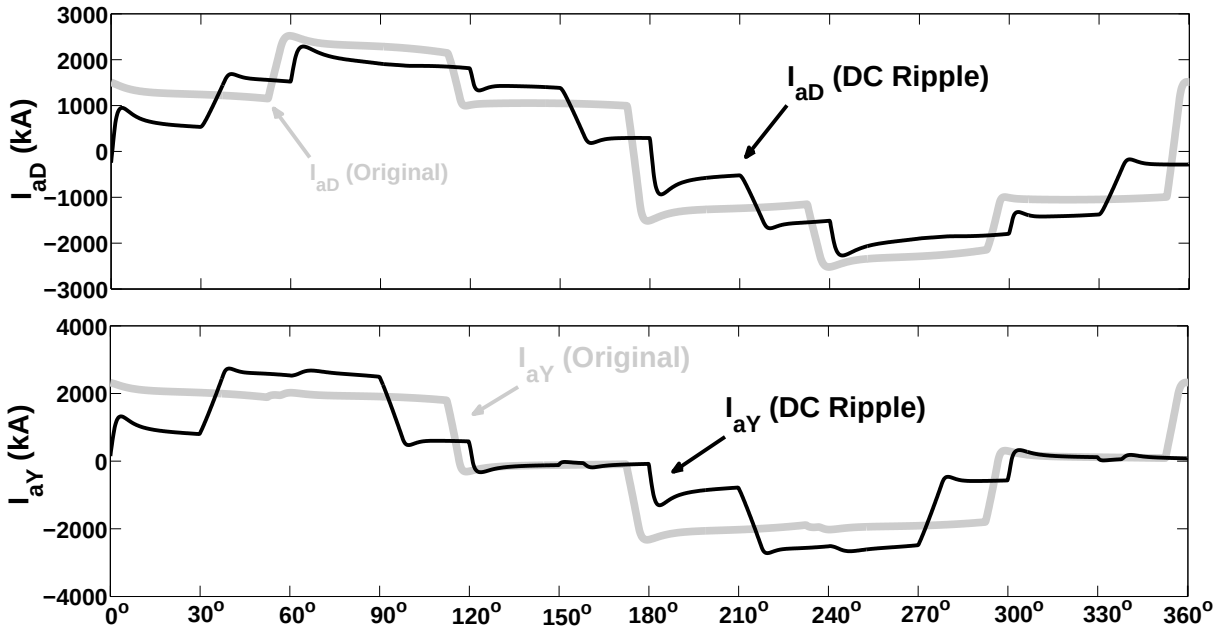


Figure 2.4: Modified I_{aD} and I_{aY} of 6-pulse converter with DC ripple reinjection.

The simulated active and reactive powers are as presented in Table. 2.3. There is a substantial increase in the reactive power demand of the converter to $Q_{sr} = 552$ MVAR when compared with $Q_{sr} = 428$ MVAR without reinjection.

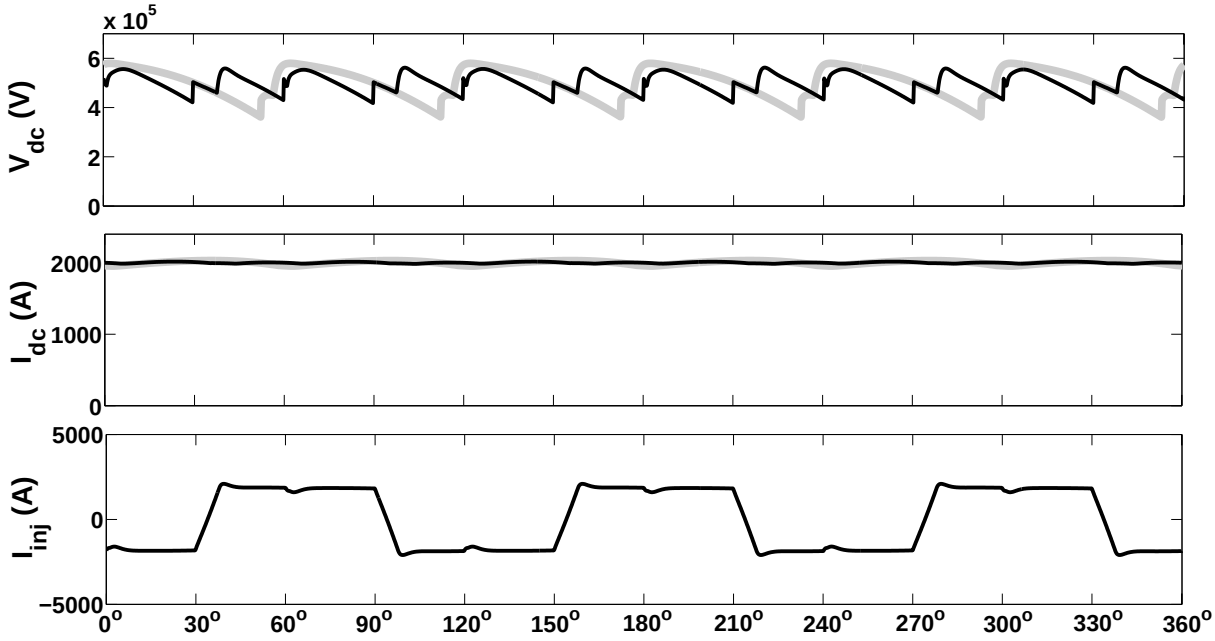


Figure 2.5: V_{dc}, I_{dc} and I_{inj} of 6-pulse converter with DC ripple reinjection.

Table 2.3: Active and Reactive Power values with DC ripple reinjection.

Simulation parameters	Value
DC power, P_{dc}	1000 MW
Source active power, P_{sr}	1000 MW
Source reactive power, Q_{sr}	552 MVAR

Although the DC ripple reinjection lowers the current and voltage THD and in spite of its relative simplicity, it is still not considered cost competitive with the use of filters due to the increased reactive power demand. Moreover, the optimization of the reinjection waveform for harmonic cancellation is not at all discussed. The injected current must contain triplen harmonics for complete harmonic elimination (to be discussed in Section 2.3).

2.2.3 12-pulse converter with DC Ripple Reinjection

The DC ripple reinjection technique is applied to transform the 12-pulse converter operation into an equivalent 24-pulse operation [Arrillaga and Villablanca 1991]. The 12-pulse rectifier with the reinjection circuit is shown in Fig. 2.6.

The firing pulses of the main converter are synchronised with the line-to-line voltage of secondary-side of the interface transformer. The converter DC voltage, V_{out}, has 12 pulses per cycle, each pulse for 30°. It is the sum of the DC bus voltages, V_a and V_b. V_a and V_b has 6 pulses per cycle which are phase shifted by 30° from each other. The output voltage, V_{out}, has 12 pulses per

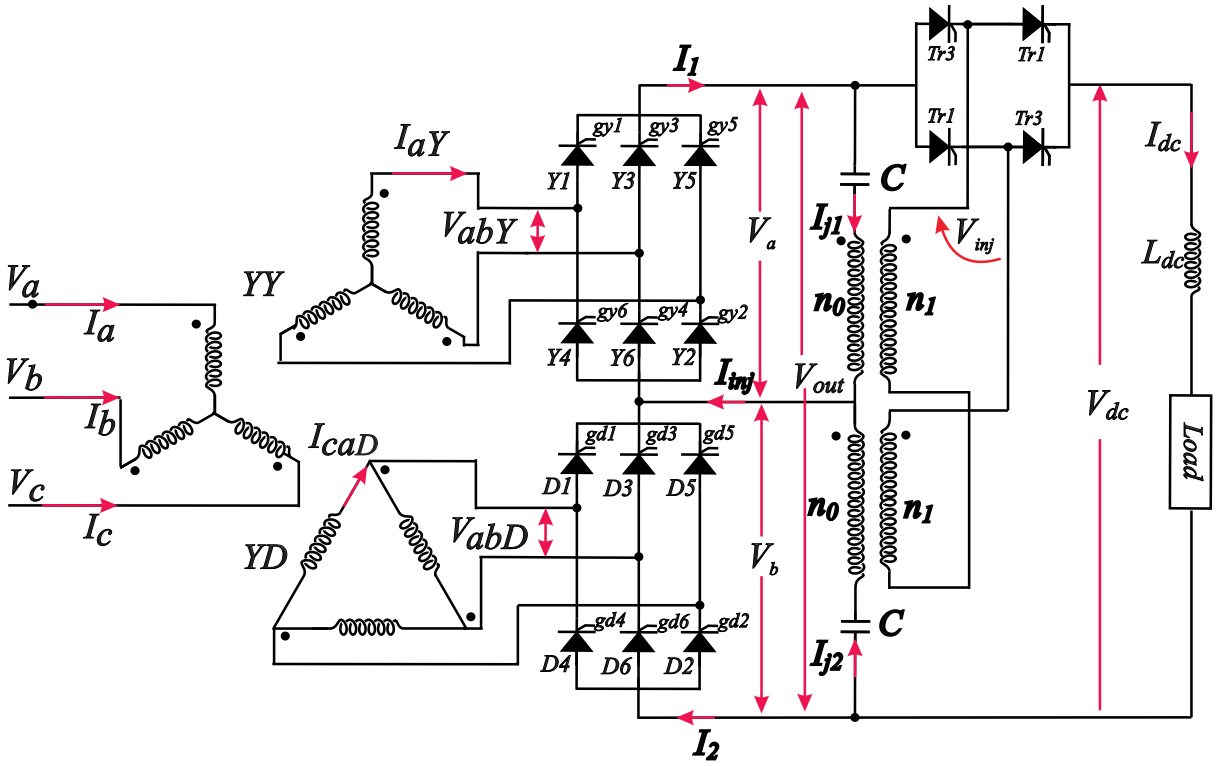


Figure 2.6: 12-pulse converter with DC ripple reinjection.

cycle, each pulse for 30°. Every new pulse in V_{out} is created by the change of the conducting state of the main rectifier. Using DC ripple reinjection, each state of the main rectifier is followed by corresponding turn-on of the reinjection thyristor pair with a delay of 15°. The synchronised firing sequence for a 12-pulse converter using DC ripple reinjection is shown in Fig. 2.7. The output DC voltage V_{dc}, has 24 pulses when compared to the 12 pulses of the 12-pulse converter.

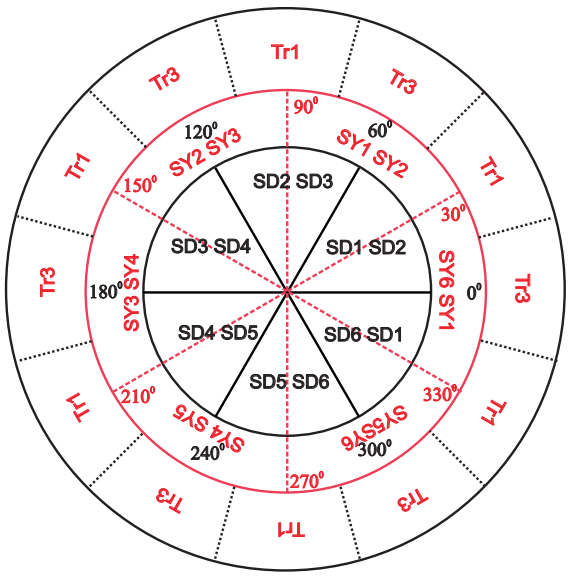


Figure 2.7: Firing sequence of 12-pulse converter with DC ripple reinjection.

The turns ratio for the reinjection transformer is [Arrillaga and Villablanca 1991]:

$$\frac{n_1}{n_0} = 0.491 \tag{2.3}$$

Reinjected current, I_{inj} with frequency six times the fundamental is injected into the mid-point of the two series connected 6-pulse converters. This modifies the AC-side line currents (the two secondary-side currents, I_{aY} and I_{caD} and primary-side current I_a). The overall THD of I_a is reduced to 7.3%, shown in Fig. 2.8. The injected currents (I_{j1}, I_{j2} and I_{inj}) are shown in Fig. 2.9. The output voltage V_{dc} and output current I_{dc} are shown in Fig. 2.10.

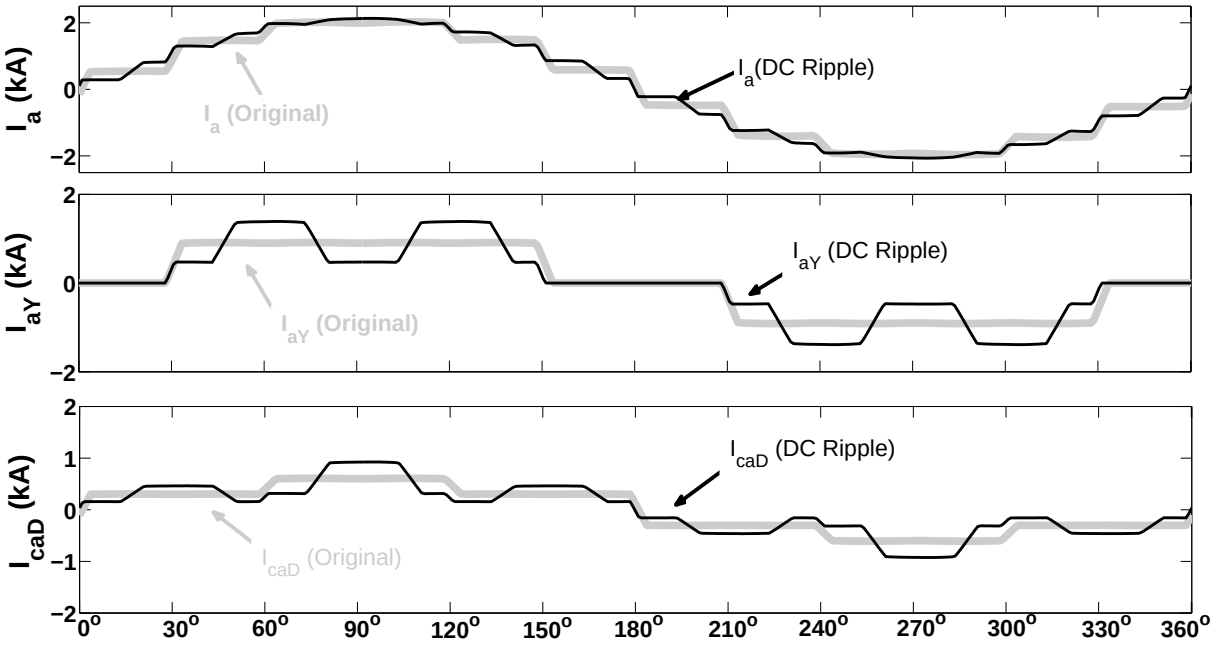


Figure 2.8: I_a, I_{aY} , I_{caD} of 12-pulse converter with DC ripple reinjection.

2.2.4 Extension of basic DC Ripple Reinjection

The use of DC ripple reinjection permitted the doubling of the pulse number of a 6-pulse converter (Section - 2.2.1) and a 12-pulse converter (Section - 2.2.2). Addition of an extra reinjection thyristor in the harmonic injector increased the pulse number from 6 to 18 [Villablanca and Arrillaga 1993] and [Arrillaga *et al.* 1993]. Similarly, the 36-pulse operation of the 12-pulse converter was confirmed in [Villablanca *et al.* 2001a] and [Villablanca *et al.* 2001b].

2.2.5 Generalisation of Basic DC Ripple Reinjection

A complete generalization of converter pulse multiplication using DC ripple reinjection is shown in Fig. 2.11 [Arrillaga *et al.* 1992] and [Villablanca *et al.* 2001c]. This generalization includes

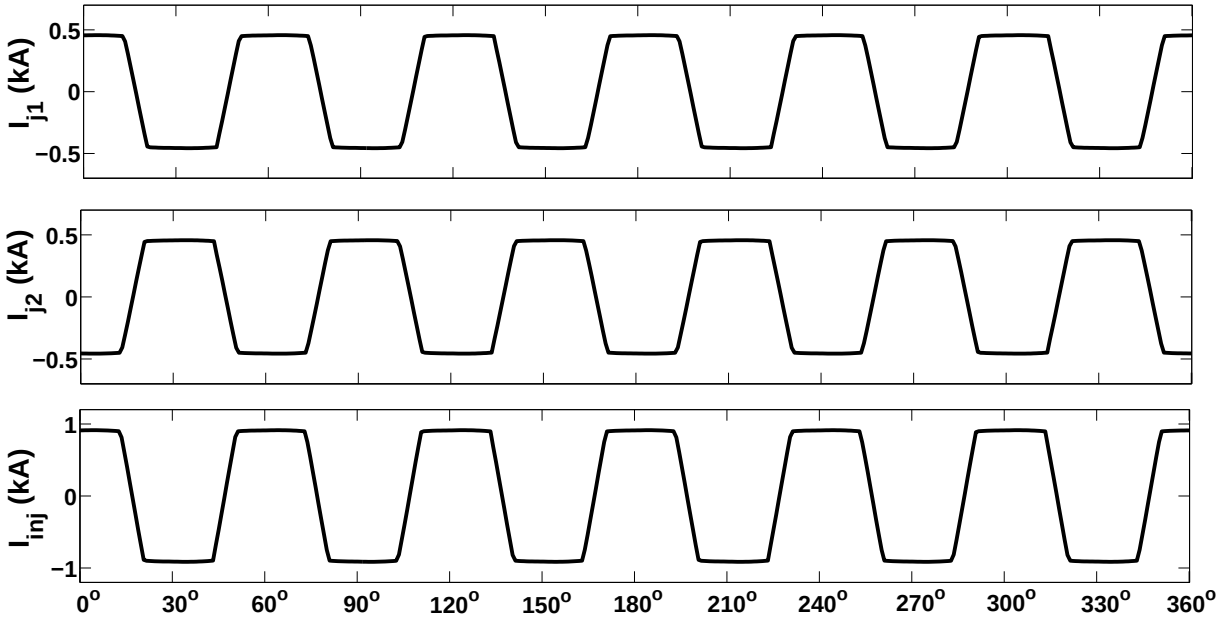


Figure 2.9: Reinjected current I_{inj} and reinjection transformer primary-side currents I_{j1} ,I_{j2}.

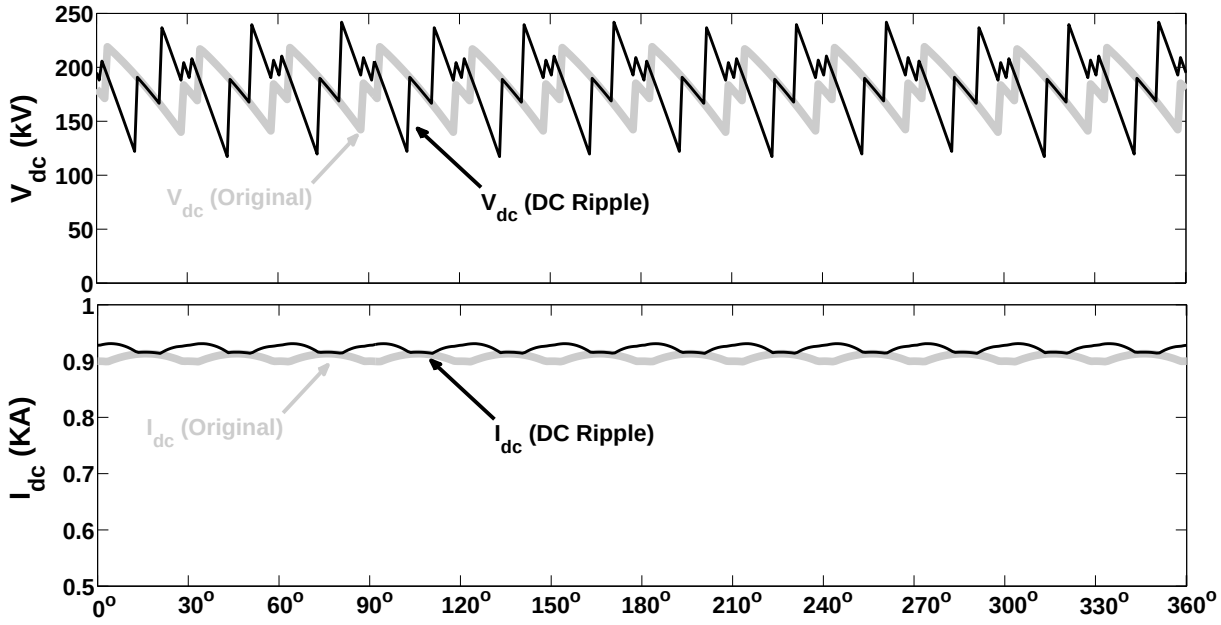


Figure 2.10: V_{dc} and I_{dc} of 12-pulse converter with DC ripple reinjection.

a rigorous phasor diagram analysis, and practicability of the schemes mentioned in preceding subsections along with their limitations.

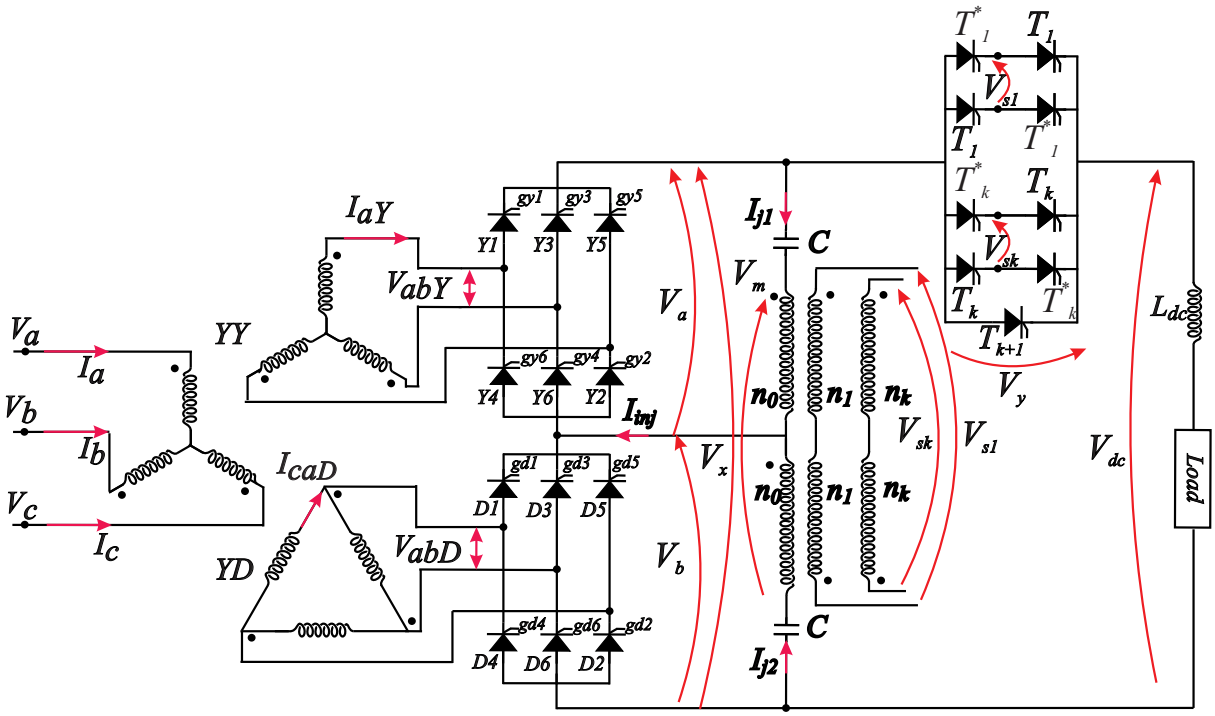


Figure 2.11: Generalisation of DC ripple reinjection for pulse multiplication in series connected rectifiers.

The following relationships hold true: $V_m = V_a - V_b$, $V_x = V_a + V_b$ and $V_{dc} = V_x + V_y$

Both the 6-pulse converters generate two signals of 'p' pulses each, which are displaced by $\theta = \pi/p$ as depicted in Fig. 2.12. The harmonic injector circuit includes 'k' single phase bridges and thyristor $T_{r(k+1)}$.

When T_k conducts:

$$V_{sk} = V_k = \frac{n_i}{n_0}(V_a - V_b) = \frac{n_i}{n_0}(V_m) \tag{2.4}$$

When T_{k+1} conducts:

$$V_{sk} = V_k = 0 \tag{2.5}$$

And when T_k^* conducts:

$$V_{sk} = V_k = -\frac{n_i}{n_0}(V_a - V_b) = -\frac{n_i}{n_0}(V_m) \tag{2.6}$$

If the triggering of the thyristors in the harmonic injector follows the timing diagram of Fig. 2.13, the following relationships hold true [Arrillaga *et al.* 1992]:

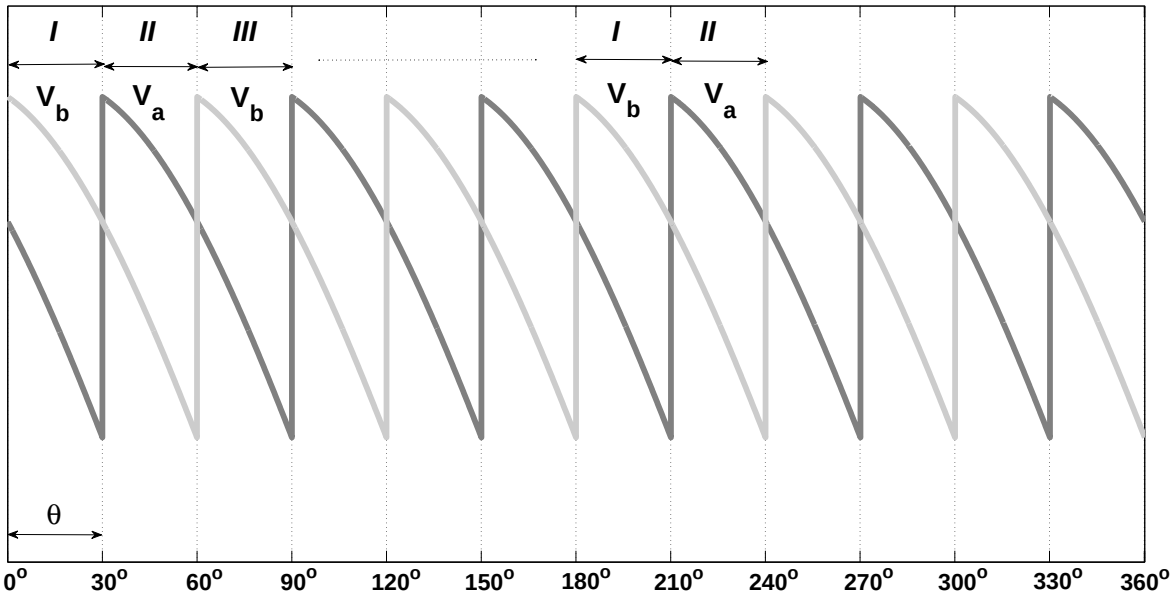


Figure 2.12: Pulse multiplication in series connected rectifiers using DC ripple reinjection.

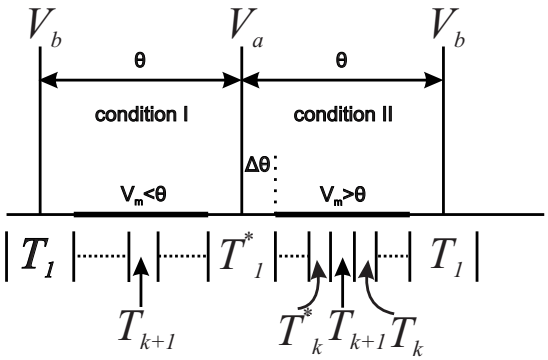


Figure 2.13: Triggering diagram of harmonic injector for pulse multiplication.

- Turns ratio of the reinjection transformer:

$$\frac{n_i}{n_0} = \frac{tan(\theta_i)}{tan(\theta/2)} \tag{2.7}$$

$$\theta_i = \frac{\pi}{Pz}\left(\frac{Pz}{2p} + 1 - 2i\right) \tag{2.8}$$

where i: 1, 2..k, Pz: final pulse number desired, p: number of pulses in V_a or V_b.

$$Pz = \begin{cases} 2p(2k+1) \\ 4pk, \qquad \text{if } T_{k+1} \text{ is omitted.} \end{cases} \tag{2.9}$$

- Minimum firing angle for natural commutation of harmonic injector circuit:

$$\alpha_{min} = \frac{\theta}{2} - \frac{2\pi}{Pz} \tag{2.10}$$

The DC ripple reinjection technique is one form of current injection which uses rectangular injection currents resulting in pulse multiplication. This basic idea was extended to higher pulse operations by addition of extra steps to the injection waveforms through extra reinjection thyristors switches. This method does not utilise the optimum injection current for complete harmonic elimination. As mentioned previously, the reactive power requirements increase with the additional harmonic injector bridge.

2.2.6 DC Ripple Reinjection using Tapped Transformer

The use of a tapped transformer to achieve pulse multiplication is proposed in [Choi *et al.* 1999], [Choi *et al.* 2000] and [Choi and Jung 2001]. Fig. 2.14 shows the 12-pulse converter with the tapped transformer T_m and auxiliary components such as DC voltage blocking capacitors C, thyristors T_1 and T_2.

V_m is the voltage across the primary winding of T_m. V_m varies with α and has six times the frequency of the line frequency. Whenever $V_m > 0$, T_1 is forward biased and is fired. This causes positive reinjection current $I_{inj} = (N_s/N_p)I_{dc}$ to be induced in the primary-side of T_m. Similarly, when $V_m < 0$, T_2 is forward biased and is fired, it induces negative reinjection current I_{inj} = -$(N_s/N_p)I_{dc}$. With turns ratio of $n_s/n_p = 0.984$, the primary-side line current (I_a) THD of 6.59% is obtained.

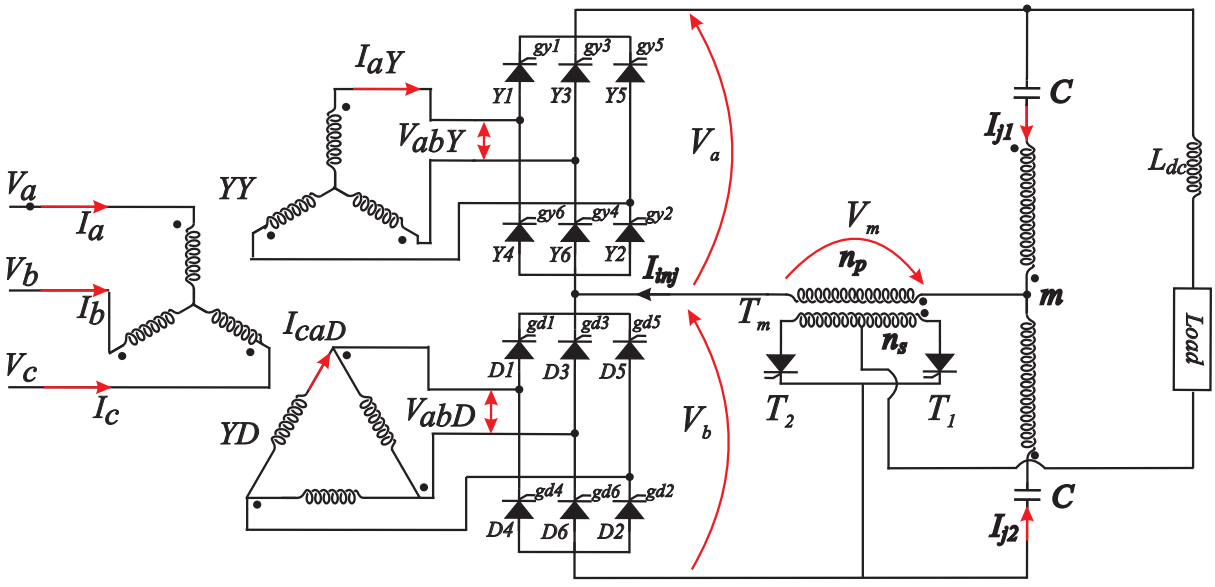


Figure 2.14: DC ripple reinjection using tapped transformer.

This method can be extended for higher pulse operation such as 36-pulse, 48-pulse, etc. using additional taps in T_m. For p-pulse operation, $p/12$ thyristors are needed. With appropriate firing angle control of the tapped thyristors, I_{inj} is a three-step waveform for 36-pulse operation and four-step waveform for 48-pulse operation. Turns ratio for 36-pulse operation is: $n_{s1}/n_p = 1.309$ while for 48-pulse operation it is: $n_{s1}/n_p = 0.977$ and $n_{s2}/n_p = 0.501$ [Choi *et al.* 2000].

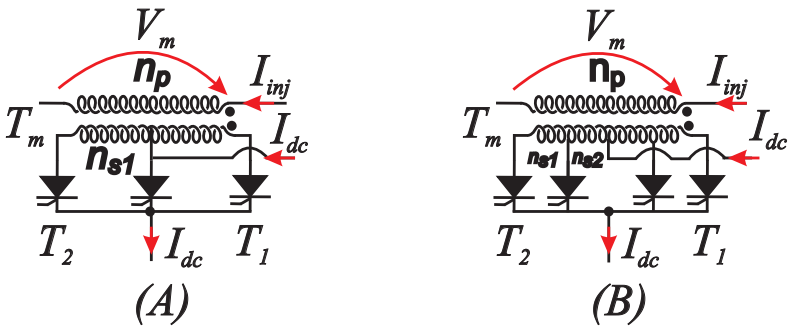


Figure 2.15: Modified harmonic injector for (A) 36-pulse operation (B) 48 pulse operation.

2.2.7 DC Ripple Reinjection using Averaging Inductor

A modified DC ripple reinjection method for series-connected rectifiers is proposed in [Xu *et al.* 2008] where an averaging inductor (L_{avg}) is used as shown in Fig. 2.16. The harmonic injector circuit uses two thyristors which is a reduction from the four reinjection thyristors used previously. This scheme can also be extended to 36 and 48-pulse operation.

With reference to Fig. 2.16, the averaging inductor is so constructed that output voltage is tapped from midpoint of the inductor. When T_{r3} conducts:

$$V_{dc} = (V_a + V_b) - \frac{1}{2} \cdot \frac{n_1}{n_0}(V_a - V_b) \tag{2.11}$$

When T_{r1} conducts:

$$V_{dc} = (V_a + V_b) + \frac{1}{2} \cdot \frac{n_1}{n_0}(V_a - V_b) \tag{2.12}$$

For p-pulse operation, the turns ratio and corresponding line current I_a THD obtained is [Xu *et al.* 2008]:

$$24 - \text{pulse} : \frac{n_1}{n_0} = 1.469, \ \text{THD} = 6.2\ \% \tag{2.13}$$

$$36 - \text{pulse} : \frac{n_1}{n_0} = 1.307, \ \text{THD} = 5.1\ \% \tag{2.14}$$

Although replacing the reinjection switches with the averaging inductor simplifies the control system, it still produces rectangular injection current to reduce the current harmonics and it does not consider the optimum I_{inj} required for complete harmonic elimination.

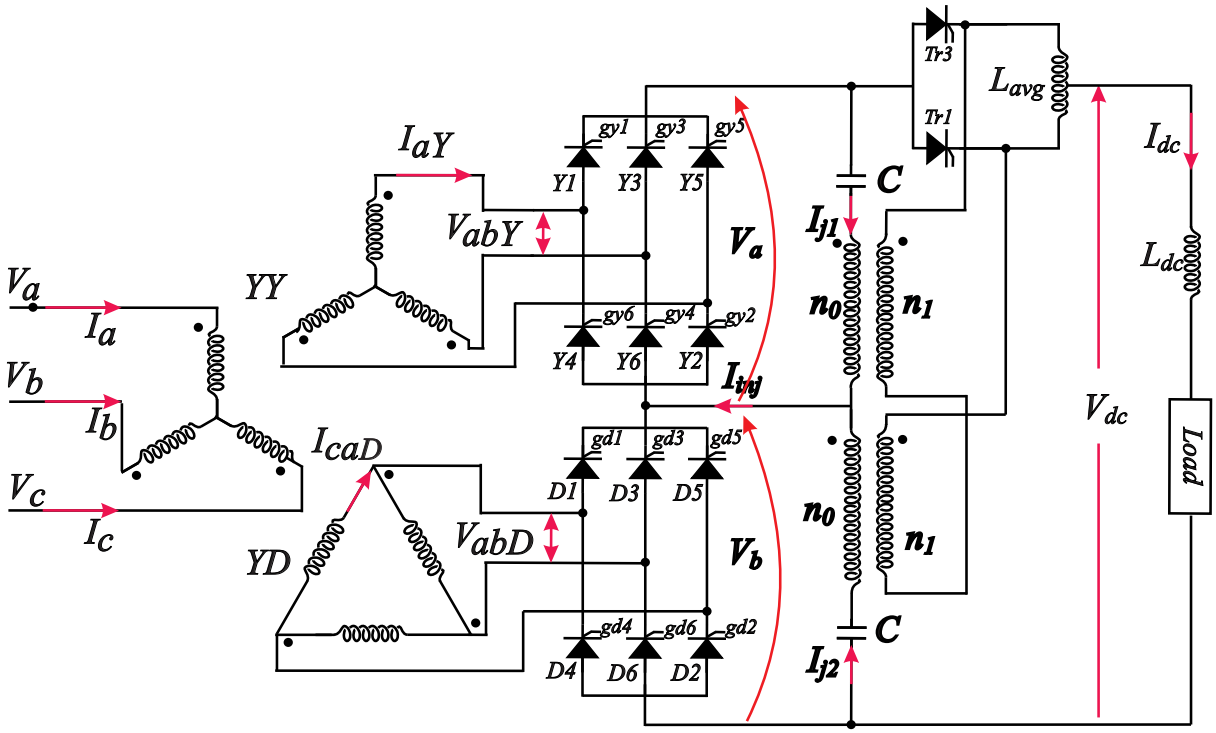


Figure 2.16: DC ripple reinjection with averaging inductor.

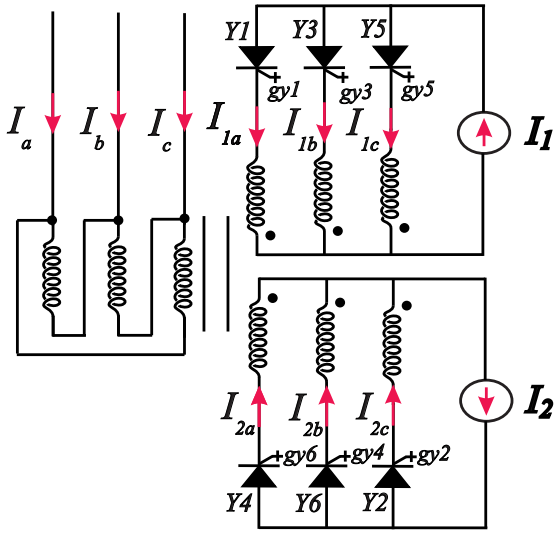


Figure 2.17: 6-pulse CSC configuration.

2.3 IDEAL INJECTION WAVEFORM: 6-PULSE CONVERTER

The mathematical justification for deriving the ideal injected current I_{inj} can be approached by treating the 6-pulse CSC as two half bridges with the interface transformer connected as D/(Y-Y) as shown in Fig. 2.17.

The currents supplied to the two half bridges from the DC current source are $I_1(\omega t)$ and $I_2(\omega t)$.

The firing sequence of the switches follows 120° switching sequence. Y1 is fired at ωt =...,-π/3, 5π/3, 11π/3,... and correspondingly Y1 switches off at ωt =...., π/3, 8π/3, 13π/3, while Y4 is fired at ωt =...,2π/3, 8π/3, 14π/3,... and correspondingly Y4 switches off at ωt =..., 4π/3, 10π/3, 16π/3,..., then currents I_{1a} and I_{2a} are given by:

$$I_{1a} = \begin{cases} 0, & -4\pi/3 < \omega t < -\pi/3 \\ I_1(\omega t), & -\pi/3 < \omega t < \pi/3 \\ 0, & \pi/3 < \omega t < 5\pi/3 \end{cases} \tag{2.15}$$

$$I_{2a} = \begin{cases} 0, & -2\pi/3 < \omega t < 2\pi/3 \\ I_2(\omega t), & 2\pi/3 < \omega t < 4\pi/3 \\ 0, & 4\pi/3 < \omega t < 8\pi/3 \end{cases} \tag{2.16}$$

If

$$I_1(\omega t) = I_{dc} + A_{1m}\cos(m\omega t) + B_{1m}\sin(m\omega t)$$

$$I_2(\omega t) = I_{dc} + A_{2m}\cos(m\omega t) + B_{2m}\sin(m\omega t)$$

then Fourier components of I_{1a} are given by:

$$I_{1an} = \int_{-\frac{\pi}{3}}^{\frac{\pi}{3}} \left[\frac{I_{dc} + A_{1m}\cos(m\omega t)}{\pi}\cos(n\omega t) + \frac{B_{1m}\sin(n\omega t)}{\pi}\sin(n\omega t)\right] d(\omega t) \tag{2.17}$$

$$= I_{dc1an} + I_{\cos 1an} + I_{\sin 1an} \tag{2.18}$$

Here

$$I_{dc1an} = \begin{cases} \frac{2I_{dc}}{n\pi}\sin\left(\frac{n\pi}{3}\right), & n = 1, 2, 3.... \\ \frac{I_{dc}}{3}(\omega t), & n = 0 \end{cases} \tag{2.19}$$

$$I_{cos1an} = \begin{cases} \frac{1}{\pi}A_{1m}\left[\frac{1}{n+m}\sin\frac{(n+m)\pi}{3} + \frac{1}{n-m}\sin\frac{(n-m)\pi}{3}\right], & m \neq n \\ \frac{1}{\pi}A_{1m}\left[\frac{1}{n+m}\sin\frac{(n+m)\pi}{3} + \frac{\pi}{3}\right], & m = n \end{cases} \tag{2.20}$$

$$I_{sin1an} = \begin{cases} \frac{1}{\pi}B_{1m}\left[\frac{1}{n-m}\sin\frac{(n-m)\pi}{3} - \frac{1}{n+m}\sin\frac{(n+m)\pi}{3}\right], & m \neq n \\ \frac{1}{\pi}B_{1m}\left[\frac{\pi}{3} - \frac{1}{n+m}\sin\frac{(n+m)\pi}{3}\right], & m = n \end{cases} \tag{2.21}$$

The following can be inferred from the above equations [Liu 2003]:

- Spectrum of I_{dc1an} does not contain harmonics of the order $n = 3l$ (l = 1, 2, 3....)

- Spectrum of I_{cos1an} depends on the frequency of $A_{1m}\cos(m\omega t)$; if $m = 3k$ ($k = 1, 2, 3...$)

$$I_{cos1an} = \begin{cases} \frac{1}{\pi}A_{1m}\left[\frac{(-1)^k}{n+3k}\sin(\frac{n\pi}{3}) + \frac{(-1)^k}{n-3k}\sin(\frac{n\pi}{3})\right] \\ = \frac{(-1)^k}{\pi}A_{1m}\frac{2n}{n^2-9k^2}\sin(\frac{n\pi}{3}), m \neq n \\ \frac{1}{\pi}A_{1m}\left[\frac{(-1)^k}{n+3k}\sin(\frac{n\pi}{3}) + \frac{\pi}{3}\right] = \frac{A_{1m}}{3}, m = n \end{cases} \tag{2.22}$$

  By choosing appropriate amplitude A_{1m} and frequency $m = 3k$, spectrum of I_{a1n} can be modified by modifying I_{cos1an}.

- Spectrum of I_{sin1an} can not affect the spectrum of I_{a1n} as all the harmonics of the same order differ by 90°.

Hence, harmonic cancellation occurs if :

$$I_{1a}(\omega t) = I_{dc} + \sum_{k=1}^{\infty} A_{1k}\cos(k\omega t) \tag{2.23}$$

$$I_{2a}(\omega t) = I_{dc} + \sum_{k=1}^{\infty} A_{2k}\cos(k\omega t) \tag{2.24}$$

And the appropriate amplitude for A_{1k} and A_{2k} is given by the explicit formula [Liu 2003]:

$$A_{1k} \approx \frac{2(-1)^k - 4}{9k^2 - 1}, \qquad k = 1, 2,... \tag{2.25}$$

$$A_{2k} \approx (-1)^k\frac{2(-1)^k - 4}{9k^2 - 1}, \qquad k = 1, 2,... \tag{2.26}$$

Fig. 2.18 illustrates the basic configuration of the current injection scheme. It is assumed that the load current, I_{dc} is constant, i.e. ripple free. It consists of the conventional 6-pulse converter with two current sources I_{j1} and I_{j2} generating a current in the neutral connection in order to modify DC bus currents as:

$$I_1 = I_{dc} + I_{j1} \tag{2.27}$$

$$I_2 = I_{dc} + I_{j2} \tag{2.28}$$

If such ideal DC bus currents $I_1(\omega t)$ and $I_2(\omega t)$ can be supplied to the two half bridges, the 6-pulse converter primary-side line current (I_{a_D}) will have no discontinuity and the THD obtained would be zero (Fig. 2.19). Some other notable contributions in this line of research (DC bus current wave-shaping) include:

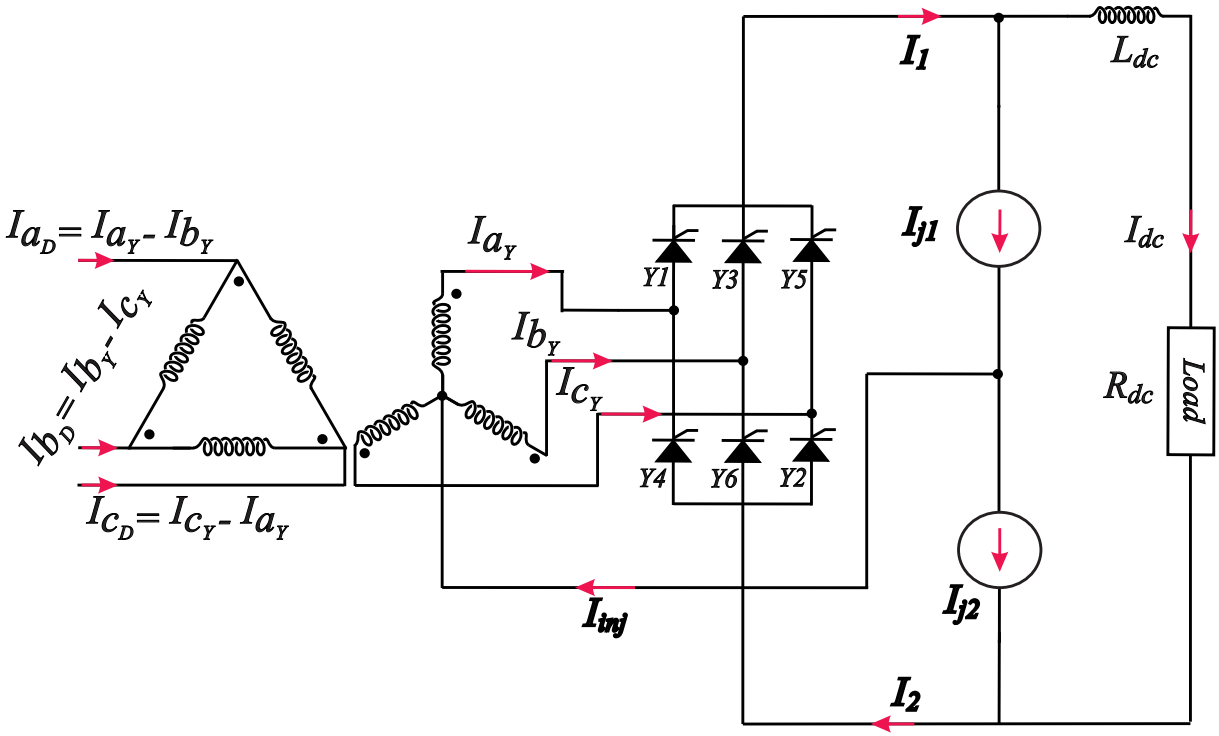


Figure 2.18: Basic configuration for harmonic current injection.

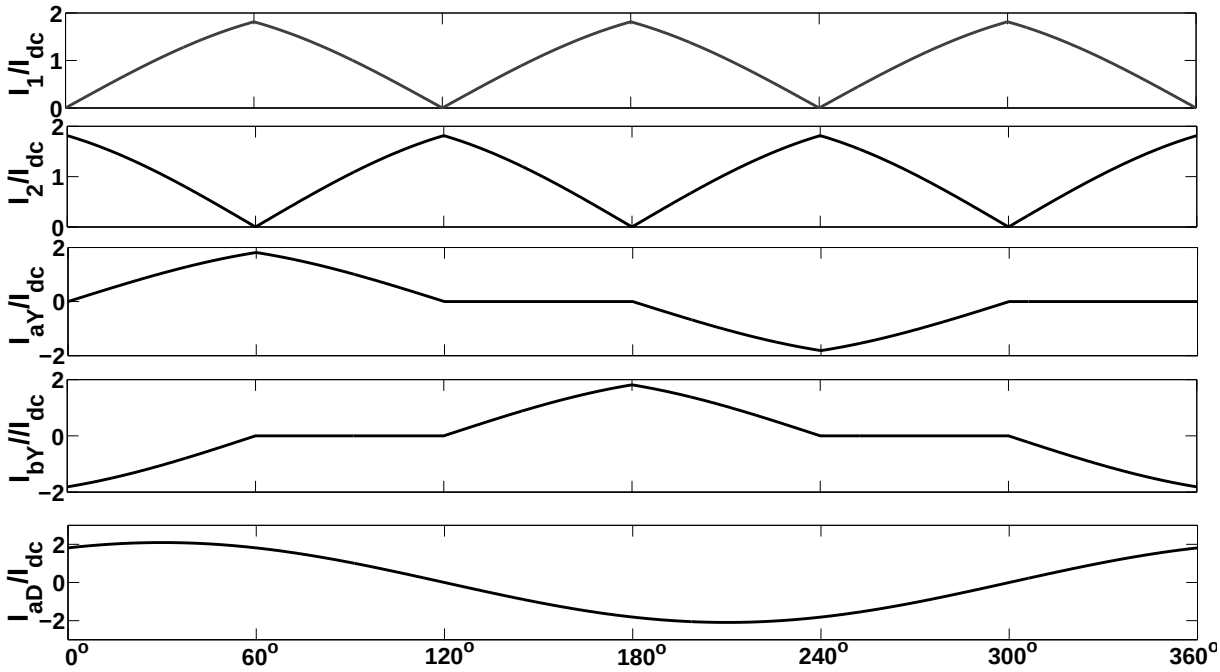


Figure 2.19: 6-pulse converter current using ideal reinjection waveform.

1. A current injection scheme where the DC bus currents are modulated by means of two Boost converters [Mohan *et al.* 1993]. The reinjection current $2{\cdot}I_{inj}$ (zero sequence injection) is injected into the AC-side of the converter by using a current injection network consisting of three LC branches, or the transformer neutral in case of a D-Y transformer. The main disadvantages of this scheme are: an increased DC-link voltage due to boost operation and the presence of diodes in series with the power flow path thereby increasing losses. 6-pulse converter primary-side line current THD of 4.3% under balanced operation is obtained.

2. A combination of a three-phase diode bridge and a DC-DC boost converter is proposed in [Kolar and Zach 1997]. The disadvantages include the boost operation, the number of elements due to the implementation of three bidirectional switches, and a complex control system.

3. A single-switch approach, using a diode converter, a boost converter and a zigzag transformer as a current injection device is used to inject I_{inj} [Hansen *et al.* 2000]. A drawback of this approach is the dependence of THD upon the value of the DC reactor. As mentioned earlier, both the DC bus currents should be individually shaped in order to draw almost sinusoidal line currents. However, the individual control of the DC bus currents cannot be implemented with this single switch approach. Line current THD = 10% is obtained using this method.

4. A scheme which considers only injecting 3rd harmonic current as I_{inj} was proposed in [Maswood 2003]. The circuit consists of a D-Y transformer as the current injector and tuned RLC circuit for generating the third-harmonic current. A bidirectional switch, added between the current shaping and current injector circuits synchronizes the injection time and thyristor gating pulse. The disadvantages include weight and cost of passive components like transformers and inductors. The line current THD is reduced to 3.8% using this method

5. Independent shaping of the DC bus currents is made possible by this scheme based on a zigzag reinjection transformer, two half-bridge inverters and two single-phase transformers [Choi *et al.* 2005]. The disadvantages of this scheme are both the high number of elements that are involved and a complex control system due to the reference signal generation. The line current THD is reduced to 2.7%.

6. Two self-commutated switches accurately shape DC bus currents following a hysteresis band [Villablanca and Nadal 2007]. When current through one switch exceeds the upper limit of the hysteresis band, it is opened and current decays through the snubber circuit. When the lower limit is exceeded of the hysteresis band, the other switch is closed, and the current starts to increase. Thus this technique can accurately shape the DC bus currents achieving primary-side line current THD of 1.1%.

2.4 CONCLUSIONS

1. The underlying principle of DC ripple reinjection is to synthesize a stepped reinjection waveform to approximate the harmonic current needed for harmonic reduction in the AC-side of the converter. This is performed by adding extra thyristors in the harmonic injector and employing the DC-side ripple voltage to realise the natural commutation for the extra thyristors. The DC ripple voltage is re-rectified and added to the DC output to improve the DC output voltage waveform.

2. The DC ripple reinjection concept is a good alternative for power quality improvement compared to filters, line reactors, etc. However, the original DC ripple reinjection concept does not synthesize the required reinjected current for complete harmonic elimination. It is also not cost competitive with harmonic filters due to the increased reactive power requirements because of the extra thyristors added to the circuit. 12-pulse, 18-pulse, 24-pulse, 36-pulse and 48-pulse equivalent high pulse converter utilising DC ripple reinjection have been reported.

3. The heart of these DC ripple reinjection converters is the magnetic component used to increase the number of pulses for reducing the line current THD and voltage ripple in DC output voltage. The major magnetic components are interface transformers on the AC-side and reinjection transformers and/or reactors on the DC-side. The rating of the interface transformer depends on load rating, with its own rating almost equal or slightly above the load rating. These transformers also provide the necessary isolation. The reinjection transformers and/or reactors are reduced in size due to their operation at higher frequency than the line frequency. Capacitors are required in the pulse multiplication circuit at output DC-side and their size and ratings are reduced with increase in the pulse number.

Chapter 3

FUNDAMENTALS OF MULTI-LEVEL CURRENT REINJECTION

3.1 INTRODUCTION

In the previous chapter, the DC ripple reinjection technique was shown as one form of current injection which used rectangular injection currents resulting in a 24-pulse operation of a 12-pulse rectifier. The basic idea was extended to higher pulse operations by the addition of extra discrete steps to the injection current through extra reinjection thyristor switches or increased reactor taps. Although higher pulse numbers were achieved, this concept was 'true' mostly for pulse doubling. This is evident from the lower order harmonics appearing in the higher pulse configurations. The reinjection waveforms were determined using phasor diagrams and graphical interpretation. The lack of mathematical explanation made the optimization of the reinjection waveform for harmonic cancellation a difficult task. Nevertheless, the DC ripple reinjection concept proved that harmonics of the modified AC-side line current and DC-side voltage waveforms are indeed reduced.

Early developments in the DC ripple reinjection concept were based on thyristors and hence the reinjection current was dependent on the line commutation condition of the thyristor. The use of thyristors was understandable, as at that time self-commutated switches were in their early days. The continued use of thyristors meant that there was the need for reactive power support.

With the advancement in the voltage and current ratings of the self-commutated switches, self-commutated switches are beginning to replace thyristor switches. Thus, dependency on the line commutation condition could be avoided if self-commutated switches are used for DC ripple reinjection. This improved reinjection concept based on optimising the current reinjection waveform to achieve harmonic suppression is termed as Multi-level Current Reinjection (MLCR).

The main difference between the traditional CSC and MLCR CSC is that the DC bus currents of the two main bridges are not constant but periodically 'varying'. This can be achieved in two different ways:

- Proper distribution of the DC current in the two main bridges. This is possible in a 12-pulse parallel bridge configuration with a multi-tapped reactor controlled by self-commutated switches.
- Addition or subtraction of an AC current to and from the DC bus current. This is possible in 12-pulse series bridge configuration where a multi-tapped reinjection transformer assists in addition and subtraction of the reinjection AC current to and from the DC bus current with the help of self-commutated switches.

The 12-pulse series configuration is used throughout this thesis. For MLCR CSC, even though the DC bus currents of the two main bridges are periodically 'varying', the converter DC current (I_{dc}) remains constant. This necessitates the use of unidirectional current passing and bidirectional voltage blocking switches in the two main bridges. This is because current always flows in the same direction for CSC whereas voltage is reversed with higher firing angle. Suitable switches include:

- IGBT plus a diode at the expense of losses and cost [Ye *et al.* 2005]. The maximum ratings available today are around 6.5 kV/2 kA.
- Reverse blocking IGBTs (RB-IGBT) have an intrinsic diode which permits reverse blocking. Power levels are still not high for now [Klumpner and Blaabjerg 2006].
- IGCTs have a semiconductor structure with low intrinsic inductance, thus allowing to shut down the current almost instantaneously. An IGCT current of 5.2 kA has been reported to turn-off within 2 μs [Suh and Steimer 2009]. This confirms the high current switching capability of IGCT in high power applications.

Section 3.2 in this chapter presents a summary of the conditions for complete elimination of harmonics in a 12-pulse CSC. For ease of understanding, all the switches and transformers are assumed to be ideal. Liu [Liu 2003] derived the Fourier components of a general 12-pulse converter bridge and concluded that the reinjection waveform should operate at six times the fundamental frequency of the AC system. After the ideal reinjection waveform which has an output with zero THD was derived, he then optimised the error square-error derivative square (ESEDS) symmetrical waveform with respect to the ideal reinjection waveform. This ESEDS waveform is closely approximated by a stepped triangular waveform using a multi-tapped reinjection transformer. The ESEDS reinjection waveform does not provide true zero current periods during main bridge commutation periods, it only approximates the zero value to a very small current close to zero.

The ideal reinjection waveform is approximated by a reinjection waveform which does provide true zero current periods. This reinjection waveform can be approximated as a linear triangle

repeated six times in a fundamental cycle. This reinjection waveform will yield slightly higher harmonic content than the ESEDS reinjection waveform [Liu 2003].

3.2 HARMONIC CANCELLATION CONCEPT

3.2.1 Basic Operation of the 12-pulse Bridge

In the MLCR-CSC, the main converter is a 12-pulse converter bridge. Fig. 3.1 shows the schematic of a 12-pulse converter bridge consisting of two three-phase full bridges and an AC interface transformer connected as Y/Y-D or D/D-Y vector group. Depending on the vector group of interface transformer, the D-connected secondary voltage may lag or lead the primary by 30° and is fired accordingly. The turns ratio of the Y-Y interface transformer is k_n:1 and the Y-D interface transformer is k_n: $\sqrt{3}$. The 120° switching scheme is used for the 12-pulse converter (Fig. 3.2).

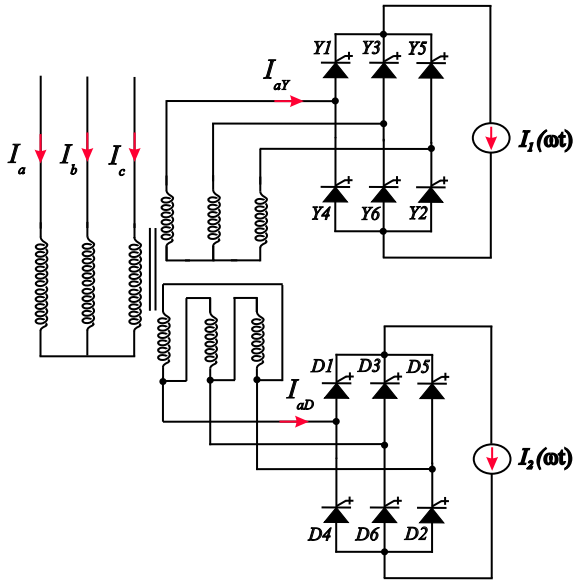
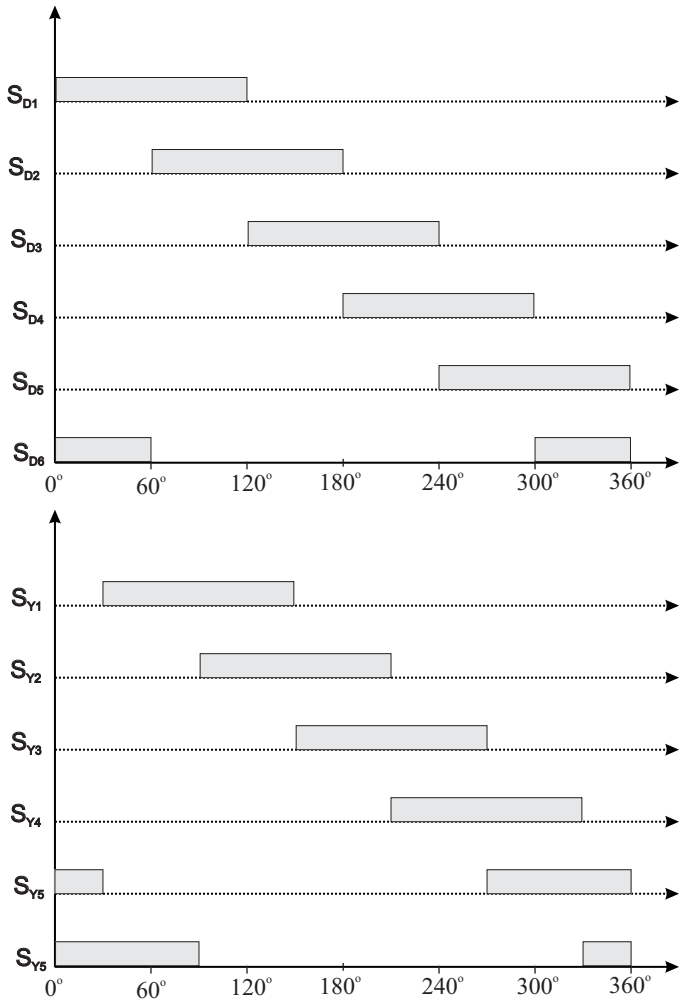


Figure 3.1: 12-pulse CSC configuration.

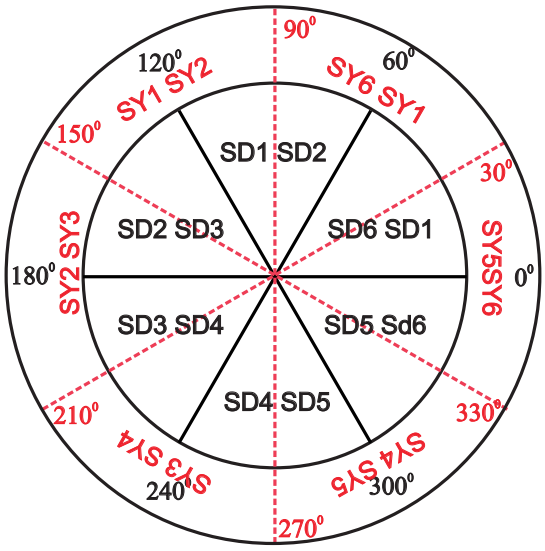
The currents supplied to the Y and D-connected bridges from their DC-sides are denoted as $I_1(\omega t)$ and $I_2(\omega t)$ respectively. Assuming a simplified case where constant DC current is applied to the bridges, i.e. $I_1(\omega t) = I_2(\omega t) = I_{dc}$, the output current waveform on one particular phase, say 'I_a' of converter phase 'A' is as shown in Fig. 3.3 where:

$$I_a(\omega t) = \frac{1}{k_n}\left[I_{aY}(\omega t) + \sqrt{3}I_{caD}(\omega t)\right] \tag{3.1}$$

The time domain components of $I_{aY}(\omega t)$ and $I_{caD}(\omega t)$ as shown in Fig. 3.3 are:



(a) 120° switching scheme of the 12-pulse bridge.



(b) Firing pattern of the 12-pulse CSC.

Figure 3.2: Firing sequence of the 12-pulse CSC.

$$I_{aY}(\omega t) = \begin{cases} 0, & 0 < \omega \mathrm{t} < \pi/6 \\ I_1(\omega t), & \pi/6 < \omega t < 5\pi/6 \\ 0, & 5\pi/6 < \omega t < 7\pi/6 \\ -I_1(\omega t), & 7\pi/6 < \omega t < 11\pi/6 \\ 0, & 11\pi/6 < \omega t < 2\pi \end{cases} \tag{3.2}$$

$$I_{caD}(\omega t) = \begin{cases} \frac{I_2(\omega t)}{3}, & 0 < \omega \mathrm{t} < \pi/3 \\ \frac{2I_2(\omega t)}{3}, & \pi/3 < \omega t < 2\pi/3 \\ \frac{I_2(\omega t)}{3}, & 2\pi/3 < \omega t < \pi \\ \frac{-I_2(\omega t)}{3}, & \pi < \omega t < 4\pi/3 \\ \frac{-2I_2(\omega t)}{3}, & 4\pi/3 < \omega t < 5\pi/3 \\ \frac{-I_2(\omega t)}{3}, & 5\pi/3 < \omega t < 2\pi \end{cases} \tag{3.3}$$

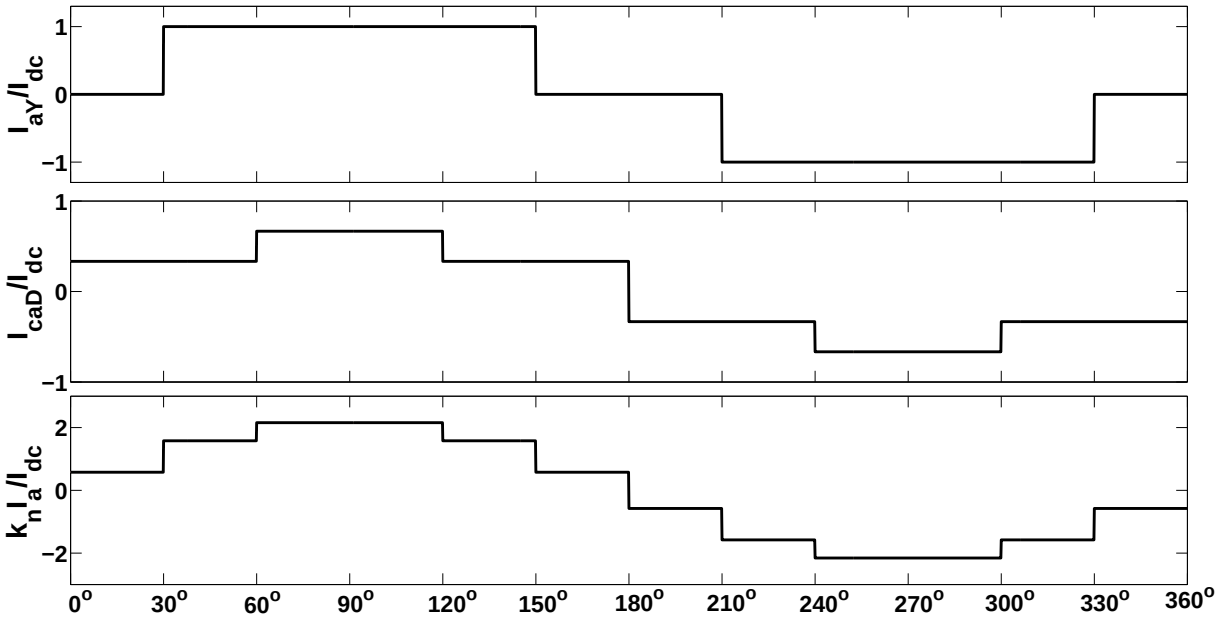


Figure 3.3: 12-pulse CSC line currents without any current reinjection.

The Fourier analysis of $I_{aY}(\omega t)$ and $I_{caD}(\omega t)$, yields harmonics of the order $n = 6l \pm 1$ ($l = 1$, 2, 3...). The magnitudes are given as:

$$I_{aY_n} = \frac{2\left[1-(-1)^n\right]}{n\pi} I_{dc} \cos\left(\frac{n\pi}{6}\right) \tag{3.4}$$

$$I_{caD_n} = \frac{4\left[1-(-1)^n\right]}{\sqrt{3}n\pi} I_{dc} \cos^2\left(\frac{n\pi}{6}\right) \tag{3.5}$$

where harmonics of the order $n = 6(2l-1)l \pm 1$ ($l = 1, 2, 3...$) of $I_{aY}(\omega t)$ and $I_{caD}(\omega t)$ are out of phase by 180° while harmonics of the order $n = 12l \pm 1$ ($l = 1, 2, 3...$) are in phase. These harmonics in phase will add constructively and penetrate into the AC system if left alone. The objective of MLCR is to inject the corresponding harmonics on the DC-side which will cancel these remaining harmonics caused by the constant DC current.

3.2.2 Harmonic elimination in 12-pulse Bridge

If the currents supplied to the Y and D-connected bridges now has a constant DC average value with some ripples:

$$I_1(\omega t) = I_{dc} + \sum_{k=1}^{\infty} A_{1k} \cos(6k\omega t) \tag{3.6}$$

$$I_2(\omega t) = I_{dc} + \sum_{k=1}^{\infty} A_{2k} \cos(6k\omega t) \tag{3.7}$$

Then as mentioned earlier, the harmonics of the order $n = 6(2l-1) \pm 1$ ($l = 1, 2, 3...$) will cancel in a 12-pulse converter, and it has been shown in [Liu 2003] that the addition of these currents in the primary-side will produce a distortion free current waveform. To obtain the ideal waveform the relation between the DC and AC components of the DC bus currents must be [Liu 2003]:

$$\sum_{k=1}^{\infty} \frac{(-1)^k A_{1k}}{(12l \pm 1)^2 - 36k^2} = \frac{I_{dc}}{(12l \pm 1)^2}, \qquad l = 1, 2,... \tag{3.8}$$

$$\sum_{k=1}^{\infty} \frac{A_{2k}}{(12l \pm 1)^2 - 36k^2} = \frac{I_{dc}}{(12l \pm 1)^2}, \qquad l = 1, 2,... \tag{3.9}$$

The condition of $(-1)^k A_{1k} = A_{2k}$ has to be fulfilled so that harmonics of order $n = 6(2l-1) \pm 1$ ($l = 1, 2, 3...$) are cancelled out by the 12-pulse bridge operation. Hence, by solving Eqn. 3.9 the solution for optimum harmonic injection in DC-side is obtained.

3.3 REINJECTION WAVEFORMS

3.3.1 Ideal Reinjection Waveforms

From the previous section, the harmonic cancellation condition can be written as:

$$\sum_{k=1}^{\infty} \frac{A_{2k}/I_{dc}}{(12l \pm 1)^2 - 36k^2} = \frac{1}{(12l \pm 1)^2}, \qquad l = 1,\ 2,... \tag{3.10}$$

which constitutes a set of linear algebraic equations for determining infinite variables (A_{2k}/I_{dc}). The numerical solutions of A_{2k} after ignoring very higher order harmonics is expressed as [Liu 2003]:

$$\frac{A_{2k}}{I_{dc}} \approx A_k \approx \frac{14.9282(-1)^k - 12.9282}{36k^2 - 1}, \qquad k = 1,\ 2,... \tag{3.11}$$

Based on the values of A_{1k} and A_{2k}, the normalised reinjection current waveforms are:

$$I_{2_{nor}}(\omega t) = 1 + \sum_{k=1}^{\infty} A_k \cos(6k\omega t) \tag{3.12}$$

$$I_{1_{nor}}(\omega t) = 1 + \sum_{k=1}^{\infty} (-1)^k A_k \cos(6k\omega t) \tag{3.13}$$

The ideal reinjection waveforms are shown in Fig. 3.4. It can be observed from the waveform that:

- Zero current values appear at those instants where the switches in the 12-pulse converter bridge commutate;
- The derivatives of the waveform are limited; particularly around the zero values where the switches in the 12-pulse converter bridge change state;
- The two waveforms, $I_1(\omega t)$ and $I_2(\omega t)$ add to a DC level with ripple.

Assuming that this ideal reinjection waveform can be supplied to the two bridges, the current waveforms of the 12-pulse converter are shown in Fig. 3.5. A pure sinusoidal line current waveform is obtained (THD = 0%) due to complete harmonic cancellation.

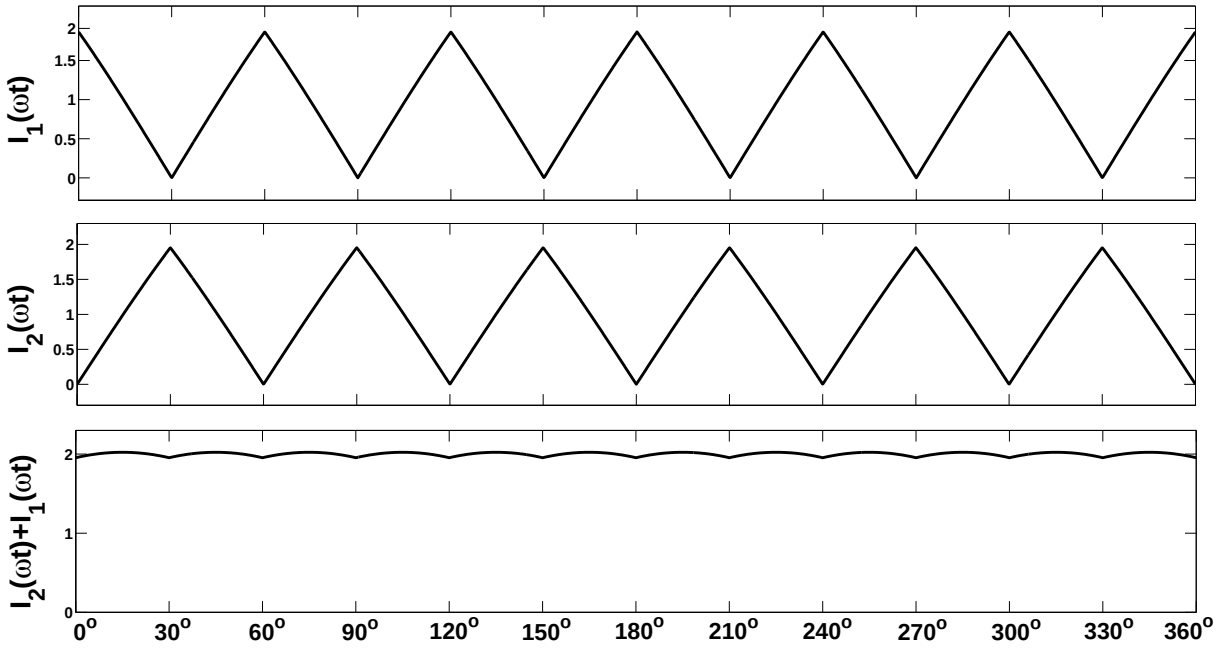


Figure 3.4: The ideal DC bus waveforms for 12-pulse CSC.

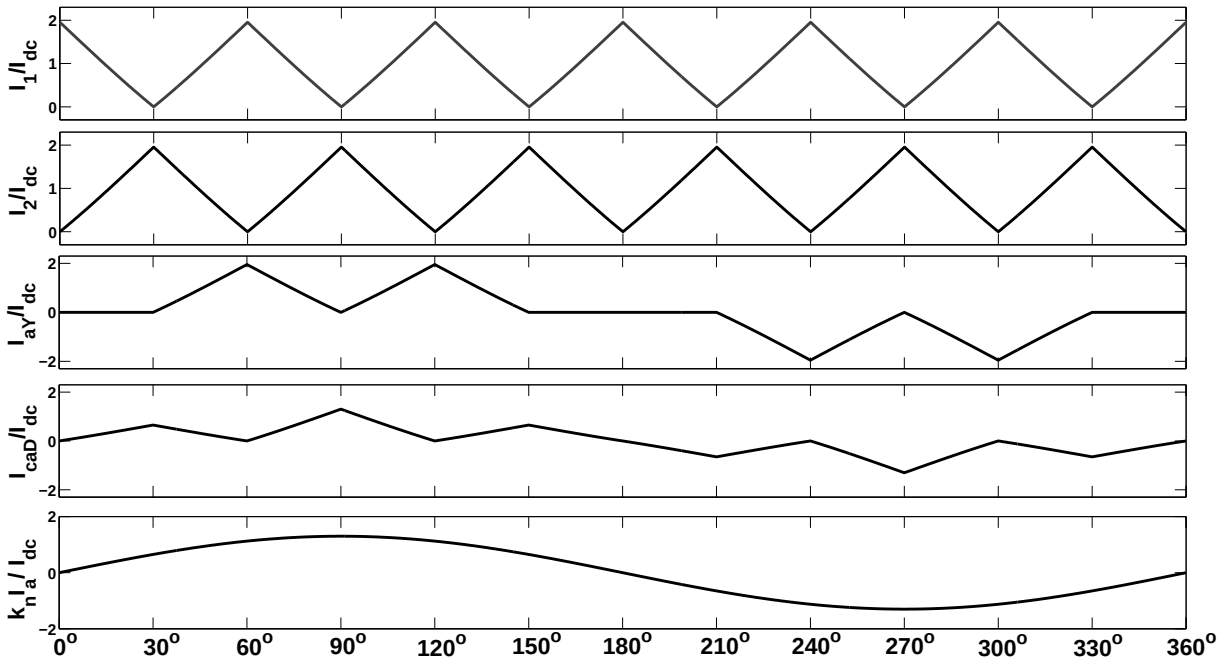


Figure 3.5: Current waveforms of 12-pulse CSC with ideal reinjection.

Practically, it is difficult to supply the two bridges with a current source of controllable ripple. Hence, a simplified approximation is needed. Liu proposed two such approximations.

3.3.2 Derived Reinjection Waveforms

The following two types of approximations are proposed [Liu 2003]:

- The ideal reinjection waveform can be approximated by a linear triangular waveform with six times the fundamental frequency. The reinjection waveform based on linearly rising and linearly falling waveforms is termed as the *linear reinjection*. The line current THD obtained with the linear reinjection waveform is 1.0553% [Liu 2003].
- A waveform which minimises the integration of *error square and the error derivative square* (ESEDS). This is the optimum approximation of the ideal reinjection waveform. Liu derived an explicit formula that yields a lesser harmonic content than the linear reinjection waveform. The line current THD obtained with the ESEDS reinjection waveform is 1.0168% [Liu 2003].

3.4 SYNTHESIS OF DERIVED REINJECTION WAVEFORMS

The proposed reinjection waveforms as described in the previous section need to be quantified into discrete levels before they can be synthesised by any practical circuit; i.e. as a multi-stepped approximation. The width and height of the multi-level reinjection steps are decided based on the following considerations:

1. simplicity of implementation, i.e. equal width and equal height steps.
2. sufficient zero width period for the power switches to switch under zero current.
3. minimum harmonic distortion caused by the multi-stepped approximation.

The ESEDS explicit formula requires that the step levels have unequal heights to generate an AC output waveform with minimum THD. The ESEDS reinjection waveform does not provide true zero current periods during main bridge commutation periods, it only approximates the zero value to a very small current, close to zero. From 0 to $\pi/6$ $[(i-1)\pi/6m$ to $i\pi/6m](i = 1, 2, ..., m)$, the width of each step is divided into m equal length portions. If the m heights are denoted by H_{si} $(i = 1, 2, ...m)$ from 0 to $\pi/6$, the step height is [Liu 2003]:

$$H_{si} = \left[1 + 14.12m \sin\left(\frac{\pi}{12}\right) \sin\left(\frac{(2i-1)\pi}{12m} - \frac{\pi}{12}\right)\right] I_{dc}, \quad i = 1,\ 2,...,\ m \tag{3.14}$$

Fig. 3.6 shows the stepped waveform approximation of ESEDS reinjection for $m = 3$. Although the zero current switching is not provided, with the increase in level number m, the level height decreases and the 12-pulse bridge switches under very low current stress. Liu demonstrated that these step levels can be generated by adding and subtracting an isolated AC current waveform to the constant DC bus current. However, the need for isolation requires the use of reinjection transformers with rigid winding restrictions. One such topology using a reinjection transformer is shown in Fig. 3.7.

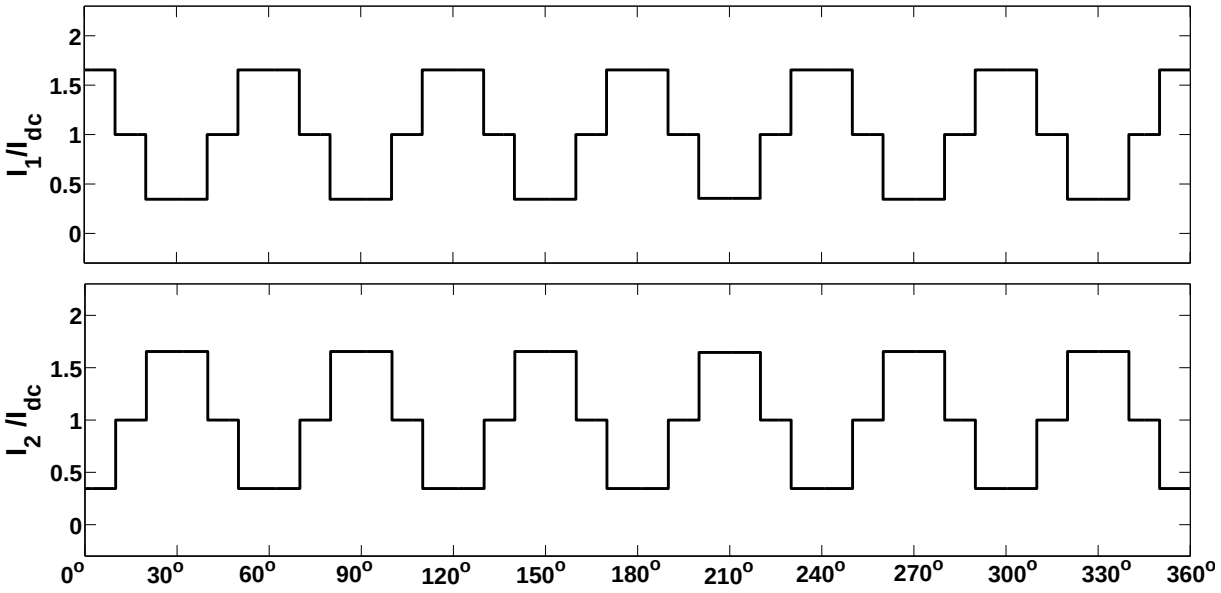


Figure 3.6: Stepped Waveform approximating ESEDS Reinjection for $m = 3$.

The triangular waveforms for linear reinjection are quantified by converting into a multi-stepped waveform of equal height and equal width. The $\pi/6$ radian interval $[-\pi/12(m-1)$ to $\pi/6 + \pi/12(m-1)](i = 1, 2, ..., m)$ is divided into *m-1* sections of equal width. The heights of the m levels are [Liu 2003]:

$$H_{Li} = \frac{2(i-1)}{m-1}, \qquad i = 1,\ 2,...,\ m \tag{3.15}$$

This stepped reinjection waveform provides true zero current periods during main bridge commutation periods as seen in Fig. 3.8. These step levels are obtained by the division of the DC

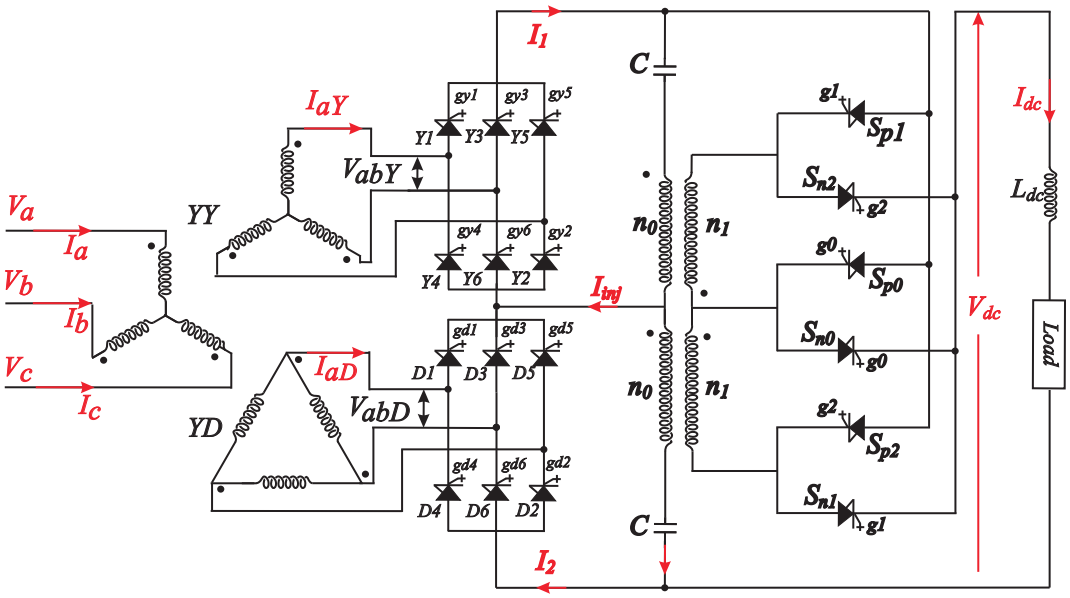


Figure 3.7: The 3-level MLCR CSC approximating ESEDS Reinjection.

current using periodically controlled multi-tapped divider. The multi-tapped divider can be a multi-tapped reactor with equal number of turns to synthesize the stepped DC bus currents I_1 and I_2. One such topology using tapped reactor is shown in Fig. 3.9.

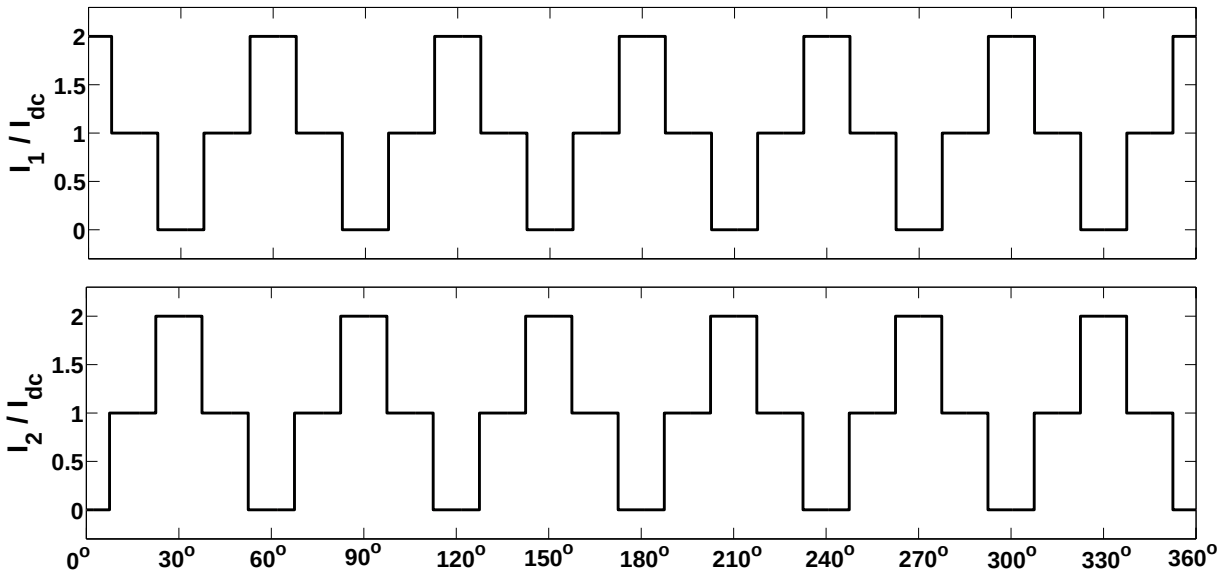


Figure 3.8: Stepped Waveform approximating Linear Reinjection for $m = 3$.

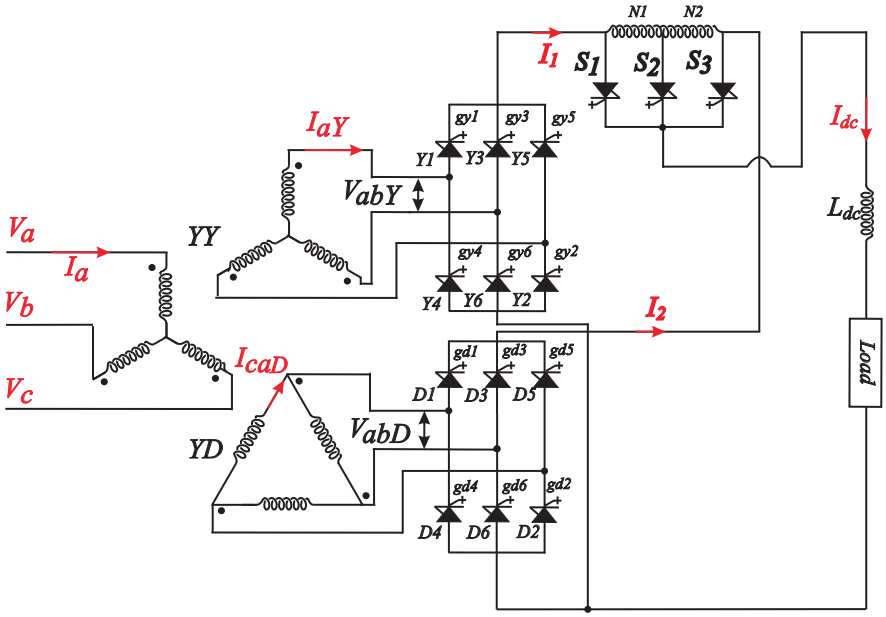


Figure 3.9: The 3-level MLCR CSC approximating Linear Reinjection.

3.5 CONCLUSIONS

1. By adopting the multi-level current reinjection concept, an AC-DC converter produces an AC current waveform which has a very low THD. The ideal reinjection waveforms are at six times the fundamental frequency and require a DC current source with variable ripple.

2. The zero values of the ideal reinjection waveform are at the same instants where the switches of the main bridges commutate indicating the possibility of achieving zero current switching.

3. Two symmetrical approximations of the ideal reinjection are: the ESEDS reinjection and linear reinjection. Both of these methods produce an AC current waveform with a very low level of 12-pulse related harmonics.

4. Linear reinjection waveform provides true zero current periods while ESEDS reinjection only approximates the zero value to a very small current. *The linear reinjection waveform will be used in this thesis to design and develop the thyristor based MLCR CSC.*

Chapter 4

THYRISTOR BASED MLCR CSC

4.1 INTRODUCTION

The linear reinjection approximation is utilised in this chapter to allow the use of thyristors in the main bridge of the 12-pulse converter. When a particular thyristor in the positive DC bus is triggered, the corresponding DC bus current I_1 is forced to be zero and none of the thyristors connected to the positive DC bus conduct (Fig. 4.1). During this time, the DC current I_{dc} flows via the auxiliary reinjection path. As I_1 is zero during commutation, it is possible to force turn-off the main bridge thyristors independently from their respective line voltages. The thyristor based MLCR CSC takes advantage of this modification and is able to achieve self-commutation as well as the ability to fire the main bridge thyristor with a negative firing angle (-α) i.e. thyristor Y1 of the Y-Y main bridge is fired at an angle α ahead of the crossing point of V_{an} and V_{cn} in their positive half cycles (Fig. 4.1). Fig. 4.2 shows line current I_a leading V_a for $-90^\circ \leq \alpha \leq 0^\circ$ using PSCAD/EMTDC results.

A comparative study, using PSCAD/EMTDC at α = -45°, is carried out for a 3-level, 5-level, and 7-level thyristor based MLCR CSC in terms of line current THD obtained, reinjection transformer requirements, reinjection switch ratings, and reinjection control circuitry complexities. Odd-levels are chosen because the addition of just one pair of extra reinjection switch adds an extra step to the stepped approximation of the varying DC current waveform. This lowers the current THD obtained compared to their even-level counterparts.

A simulation study, using PSCAD/EMTDC, is also included to study the influence of RCD snubber across the reinjection switches on the performance of 3-level thyristor based MLCR CSC.

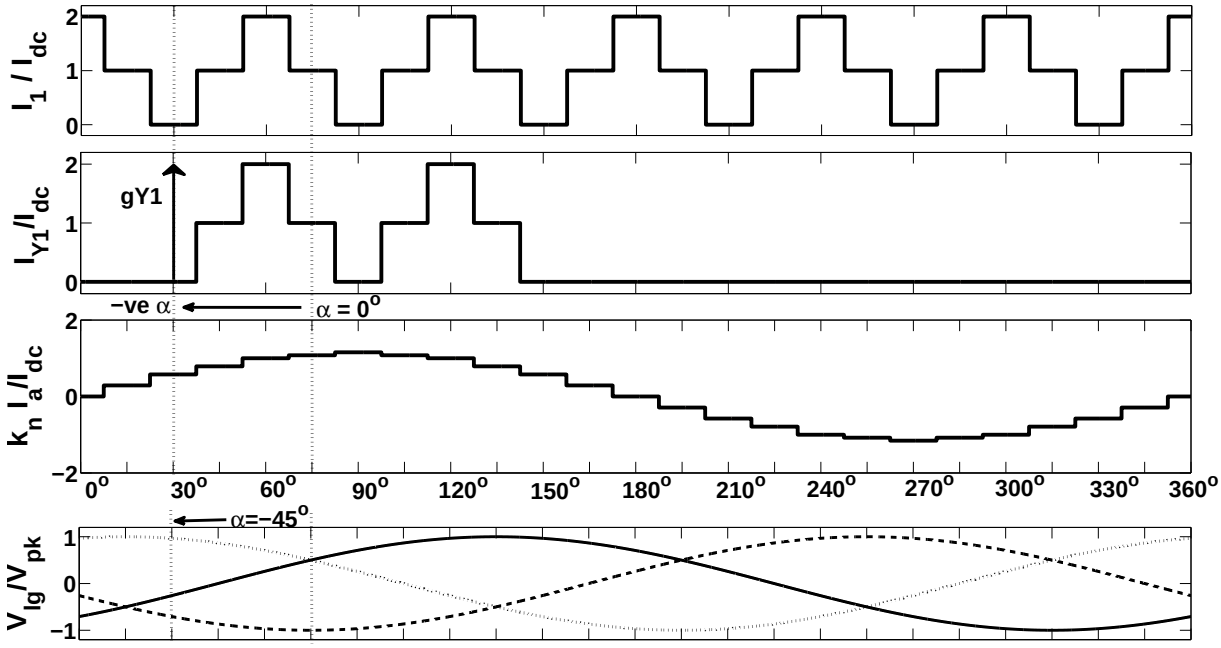


Figure 4.1: Negative firing angle waveforms for a 3-level Thyristor based MLCR CSC.

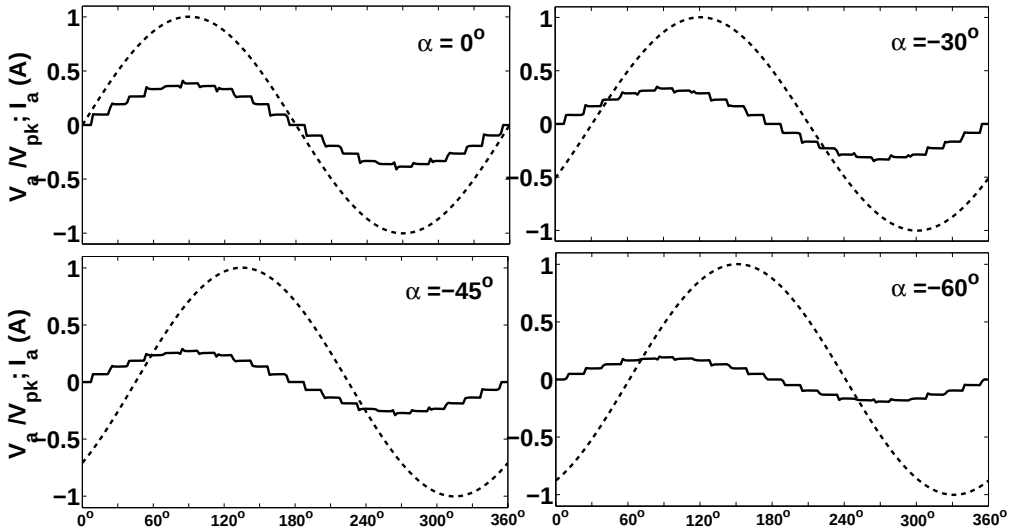


Figure 4.2: V_a and I_a for 3-level thyristor based MLCR CSC with different firing angles.

4.2 3-LEVEL THYRISTOR BASED MLCR CSC

Fig. 4.3 shows the 3-level thyristor based MLCR CSC along with the reinjection circuit. The primaries of the two single-phase transformers are connected across the DC bus through DC blocking capacitors (C). The DC current (I_{dc}) flows through the reinjection IGBTs, smoothing inductance (L_{dc}) and the load (R_{dc}). It is chopped into an AC waveform in the secondary winding of the reinjection transformer with the help of reinjection switches (S_{p1}/S_{n1} etc). These

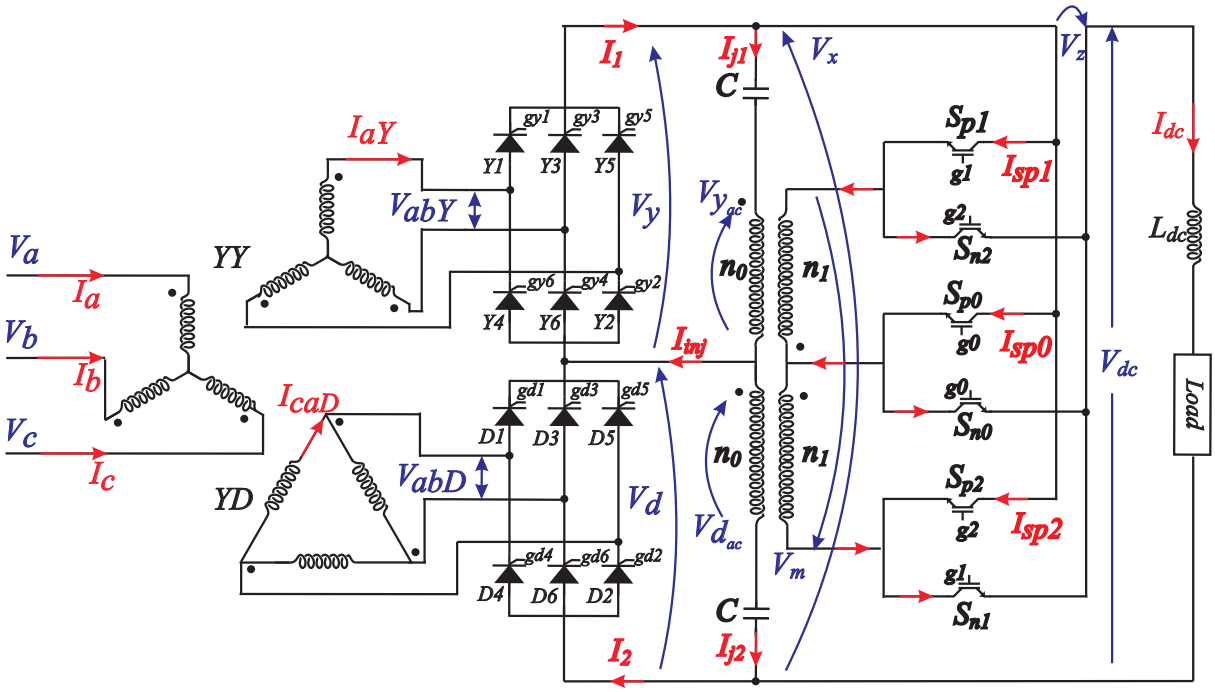


Figure 4.3: 3-level Thyristor based MLCR CSC with Linear Reinjection.

Table 4.1: Reinjection Switching Combinations and 3-level Reinjection Current.

On-state switches	I_{j1}	I_1	I_{j2}	I_2
Sp1/Sn1	I_{dc}	$2I_{dc}$	-I_{dc}	0
Sp0/Sn0	0	I_{dc}	0	I_{dc}
Sp2/Sn2	-I_{dc}	0	I_{dc}	$2I_{dc}$

currents are coupled to the reinjection transformer primary winding to form multi-level currents I_{j1} and I_{j2} which combine to form reinjection current I_{inj}. I_{inj} shapes the DC bus currents I_1 and I_2 into multi-level waveforms. The reinjection circuit generates three current steps in I_1 and I_2. Two levels are generated due to reverse connected switches (S_{p1}/ S_{n1} and S_{p2}/ S_{n2}) and one additional level is obtained by firing S_{p0}/ S_{n0} when I_{j1} and I_{j2} are both zero. Table 4.1 shows the corresponding relationship between I_1 and I_2, I_{j1} and I_{j2} with the corresponding reinjection switch ON-state. The reinjection transformer is a single-phase two-winding transformer with transformer turns ratio (c.f. Fig. 4.3):

$$\frac{n_1}{n_0} = 1 \tag{4.1}$$

The angular sequence (β_i) for the reinjection switching sequence (repeats every $\frac{\pi}{6}$ radians) is (c.f. Fig. 4.15):

$$\beta_i = \frac{(2i-1)\pi}{24}, \text{ where } i = 1, 2. \tag{4.2}$$

4.2.1 AC-side Current Waveforms

From the time domain components of the currents $I_{aY}(\omega t)$ and $I_{caD}(\omega t)$ as given in Appendix A and with reference to Fig. 4.3, the primary-side AC line current $I_a(\omega t)$ is:

$$I_a(\omega t) = \frac{1}{k_n}\left[I_{aY}(\omega t) + \sqrt{3}I_{caD}(\omega t)\right] \tag{4.3}$$

where k_n: turns ratio of the main transformer.

The Fourier components of the secondary-side AC line currents $I_{aY}(\omega t)$ and $I_{caD}(\omega t)$ are:

$$\begin{aligned} I_{aY_n} &= \frac{2}{\pi}\int_0^{\pi} I_{aY}\sin(n\omega t)d(\omega t) \\ &= \frac{16[1-(-1)^n]I_{dc}}{2n\pi}\sin\left(\frac{n\pi}{24}\right)\cos\left(\frac{n\pi}{6}\right)\left[2\sin\left(\frac{n\pi}{6}\right)+\sin\left(\frac{n\pi}{3}+\frac{n\pi}{12}\right)\right] \end{aligned} \tag{4.4}$$

$$\begin{aligned} I_{caD_n} &= \frac{2}{\pi}\int_0^{\pi} I_{caD}\sin(n\omega t)d(\omega t) \\ &= \frac{16[1-(-1)^n]I_{dc}}{6n\pi}\sin\left(\frac{n\pi}{24}\right)\cos\left(\frac{n\pi}{6}\right)\left[2\sin\left(\frac{n\pi}{3}\right)+2\cos\left(\frac{n\pi}{6}\right)\sin\left(\frac{n\pi}{3}+\frac{n\pi}{12}\right)\right] \end{aligned} \tag{4.5}$$

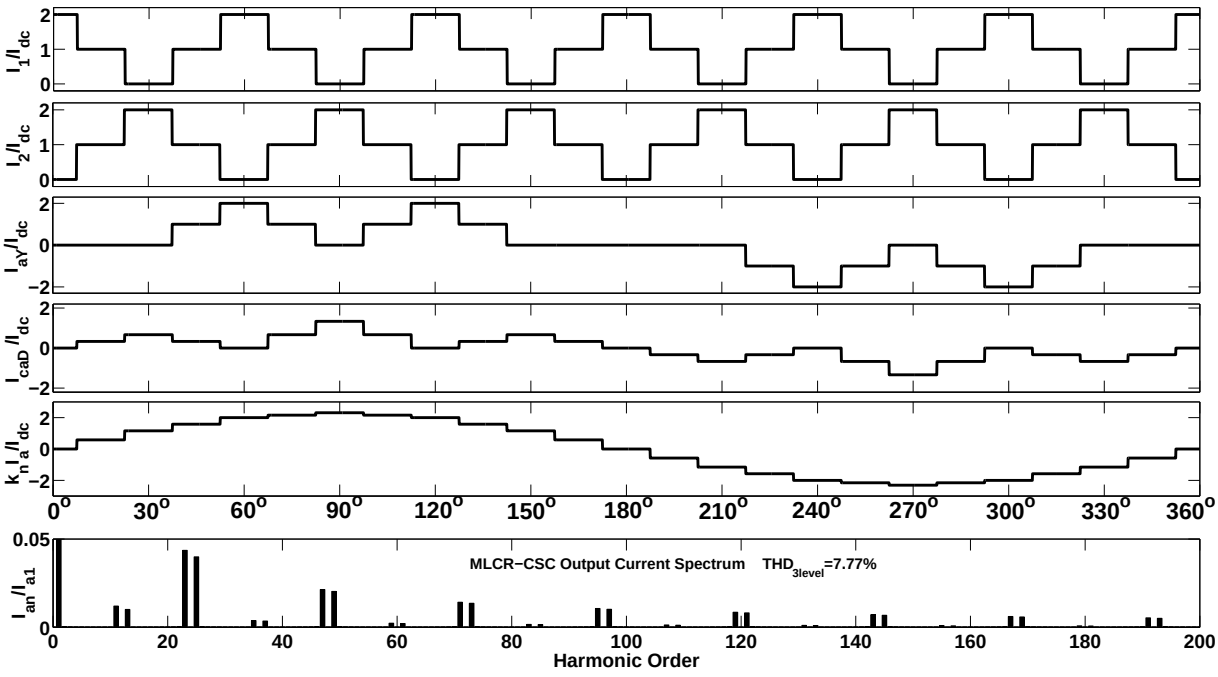


Figure 4.4: Current waveforms for 3-level thyristor based MLCR CSC with Linear Reinjection.

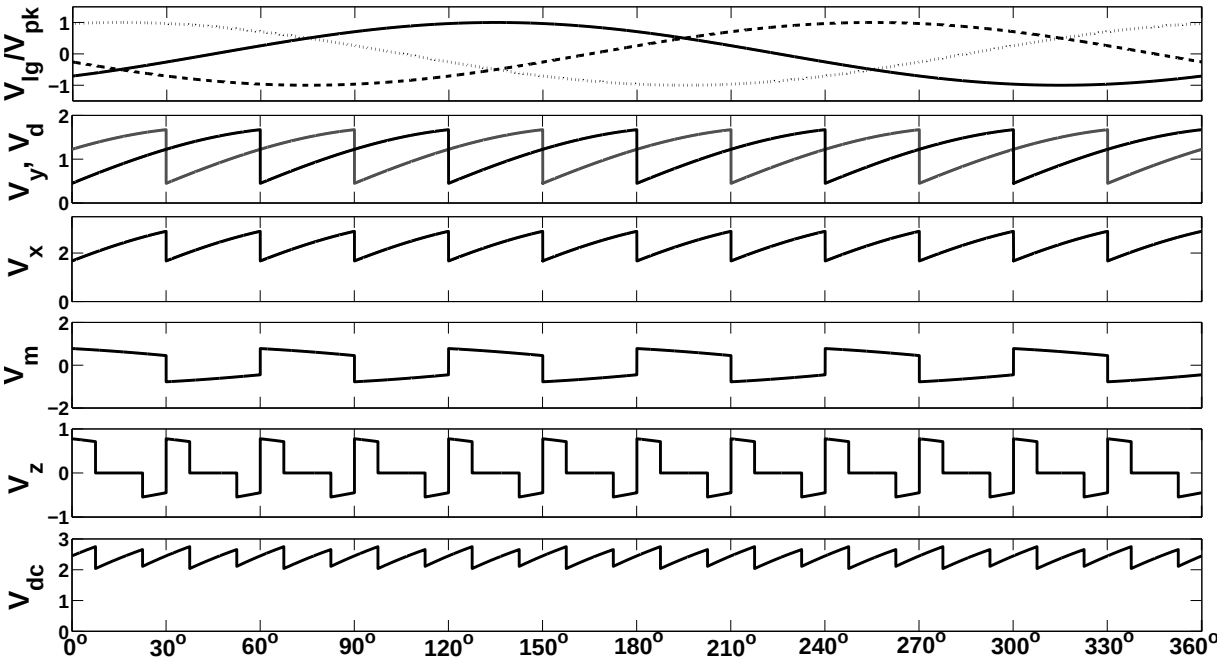


Figure 4.5: Theoretical DC voltage waveforms for 3-level thyristor based MLCR CSC for α = -45°.

The various current waveforms are shown in Fig. 4.4. The peak value (I_{a1}) of the fundamental component of I_a is derived from Eqns. (4.3), (4.4) and (4.5) and is:

$$\begin{aligned} I_{a1} &= \frac{32\sqrt{3}I_{dc}}{2k_n\pi}\sin\left(\frac{\pi}{24}\right)\left[1+\sin\left(\frac{\pi}{3}+\frac{\pi}{12}\right)\right] \\ &\simeq \frac{2.26323}{k_n}I_{dc} \end{aligned} \tag{4.6}$$

The RMS value of I_a is:

$$\begin{aligned} I_{arms} &= \sqrt{\frac{1}{\pi}\int_0^{\pi} I_a(\omega t)^2 d(\omega t)} \\ &= \frac{1.6054}{k_n}I_{dc} \end{aligned} \tag{4.7}$$

THD derived is therefore:

$$\text{THD} = \sqrt{\left(\frac{I_{a_{rms}}}{I_{a1_{rms}}}\right)^2 - 1} \tag{4.8}$$

By using Eqns. (4.6), (4.7) and (4.8), $\text{THD}_{3level} = 7.77\%$. The harmonic spectrum of I_a is also shown in Fig. 4.4.

4.2.2 DC-side Voltage Waveforms

The DC-side voltage waveforms are time referenced with respect to the AC-side current waveform I_a (Fig. 4.4). The DC-side voltages across the individual bridges ($V_y(\omega t)$ and $V_d(\omega t)$) are related to the converter-side phase voltages of the Y-Y and Y-D connected bridges and switching functions f_{sY} and f_{sD} as:

$$V_y(\omega t) = f_{sY}\frac{1}{k_n}\begin{bmatrix} V_a(\omega t) & V_b(\omega t) & V_c(\omega t)\end{bmatrix}^T \tag{4.9}$$

$$V_d(\omega t) = f_{sD}\frac{1}{k_n}\begin{bmatrix} V_a(\omega t+\pi/6) & V_b(\omega t+\pi/6) & V_c(\omega t+\pi/6)\end{bmatrix}^T \tag{4.10}$$

where

$$f_{sY}(\omega t) = \begin{cases} [0 \quad -1 \quad 1] & 0 < \omega t < \frac{\pi}{6} \\ [1 \quad -1 \quad 0] & \frac{\pi}{6} < \omega t < \frac{\pi}{2} \\ [1 \quad 0 \quad -1] & \frac{\pi}{2} < \omega t < \frac{5\pi}{6} \\ [0 \quad 1 \quad -1] & \frac{5\pi}{6} < \omega t < \frac{7\pi}{6} \\ [-1 \quad 1 \quad 0] & \frac{7\pi}{6} < \omega t < \frac{9\pi}{6} \\ [-1 \quad 0 \quad 1] & \frac{9\pi}{6} < \omega t < \frac{11\pi}{6} \\ [0 \quad -1 \quad 1] & \frac{11\pi}{6} < \omega t < 2\pi \end{cases} \qquad f_{sD}(\omega t) = \begin{cases} [1 \quad -1 \quad 0] & 0 < \omega t < \frac{\pi}{3} \\ [1 \quad 0 \quad -1] & \frac{\pi}{3} < \omega t < \frac{2\pi}{3} \\ [0 \quad 1 \quad -1] & \frac{2\pi}{3} < \omega t < \pi \\ [-1 \quad 1 \quad 0] & \pi < \omega t < \frac{4\pi}{3} \\ [-1 \quad 0 \quad 1] & \frac{4\pi}{3} < \omega t < \frac{5\pi}{3} \\ [0 \quad -1 \quad 1] & \frac{5\pi}{3} < \omega t < 2\pi \end{cases} \tag{4.11}$$

Based on the above switching functions, $V_y(\omega t)$ and $V_d(\omega t)$ are plotted in Fig. 4.5 with respect to the peak phase source voltage (V_{pk}) and can be expressed as for the first $\pi/6$ interval as:

$$V_y(\omega t) = \frac{\sqrt{3}}{k_n}V_{pk}\cos(\omega t + \alpha) \tag{4.12}$$

$$V_d(\omega t) = \frac{\sqrt{3}}{k_n}V_{pk}\cos(\omega t + \alpha - \frac{\pi}{6}) \tag{4.13}$$

$$V_x(\omega t) = V_y(\omega t) + V_d(\omega t) \tag{4.14}$$

With reference to Fig. 4.3, the voltage V_m across the reinjection transformer is:

$$V_m(\omega t) = \left[V_{y_{ac}(\omega t)} - V_{d_{ac}(\omega t)}\right] \tag{4.15}$$

$$\approx [V_y(\omega t) - V_d(\omega t)] \tag{4.16}$$

The DC load voltage (V_{dc}) is calculated as:

$$V_{dc}(\omega t) = V_x(\omega t) + V_z(\omega t) \tag{4.17}$$

When the i^{th} pair of reinjection IGBT S_{pi}/S_{ni} (i = 0, 1, 2) is switched on, then voltage $V_z(\omega t)$ is given by:

$$V_z(\omega t) = \begin{cases} V_m(\omega t), & 0 \leq \omega t \leq \frac{\pi}{24} \\ 0, & \frac{\pi}{24} \leq \omega t \leq \frac{3\pi}{24} \\ -V_m(\omega t), & \frac{3\pi}{24} \leq \omega t \leq \frac{5\pi}{24} \\ 0, & \frac{5\pi}{24} \leq \omega t \leq \frac{7\pi}{24} \\ V_m(\omega t), & \frac{7\pi}{24} \leq \omega t \leq \frac{\pi}{3} \end{cases} \tag{4.18}$$

From Fig. 4.5 it can be seen that there are 2 voltage pulses for every 30°. Therefore the average V_{dc} is calculated from:

$$V_{dc} = \frac{6}{\pi} \sum_{i=1}^{2} \int_{\frac{(2i-3)\pi}{24}}^{\frac{(2i-1)\pi}{24}} V_x(\omega t) + V_z(\omega t) \tag{4.19}$$

The average V_{dc} obtained by solving Eqn. (4.19) is:

$$\begin{aligned} V_{dc} &= \frac{48\sqrt{3}V_{pk}}{2\pi k_n} \sin\left(\frac{\pi}{24}\right) \left[1 + \sin\left(\frac{\pi}{3} + \frac{\pi}{12}\right)\right] \cos(\alpha) \\ &\approx 3.39 \frac{V_{pk}}{k_n} \cos(\alpha) \end{aligned} \tag{4.20}$$

The harmonic spectrum of V_{dc} is shown in Fig. 4.6. It can be clearly seen that the dominant harmonics are the 24^{th}, 48^{th}, 72^{nd}, 96^{th}, and 120^{th} which represents a 24-pulse operation. Small amounts of 12-pulse related harmonics such as 12^{th}, 36^{th}, 60^{th}, etc. can also be seen but the magnitude is negligible.

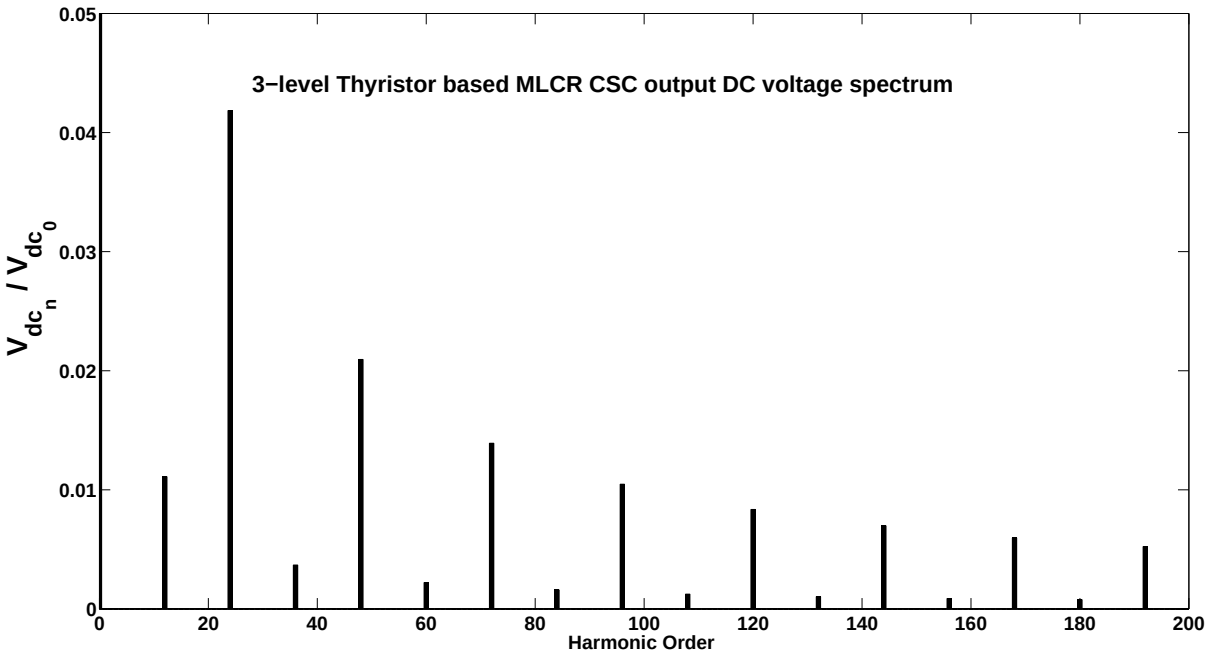


Figure 4.6: Harmonic spectrum of V_{dc} of a 3-level thyristor based MLCR CSC for α = -45°.

Table 4.2: Reinjection Switching Combinations and 5-level Reinjection Current.

On-state switches	winding	I_{j1}	I_1	I_{j2}	I_2
Sp1/Sn1	n_0:$n_1 + n_2$	I_{dc}	$2I_{dc}$	-I_{dc}	0
Sp2/Sn2	n_0:n_2	$0.5I_{dc}$	$1.5I_{dc}$	-$0.5I_{dc}$	$0.5I_{dc}$
Sp0/Sn0	0	0	I_{dc}	0	I_{dc}
Sp3/Sn3	n_0:n_2	-$0.5I_{dc}$	$0.5I_{dc}$	$0.5I_{dc}$	$1.5I_{dc}$
Sp4/Sn4	n_0:$n_1 + n_2$	-I_{dc}	0	I_{dc}	$2I_{dc}$

4.3 5-LEVEL THYRISTOR BASED MLCR CSC

Fig. 4.7 shows the configuration for 5-level MLCR CSC. The 5-level MLCR CSC works in a similar manner to the 3-level MLCR CSC. Table 4.2 shows the corresponding relationship between I_1 and I_2, I_{j1} and I_{j2} with the corresponding reinjection switch ON-state. The reinjection transformer is a single-phase three-winding transformer with turns ratio of (c.f. Fig. 4.7):

$$\frac{n_2}{n_0} = 0.5 \text{ and } \frac{n_1}{n_0} = 0.5 \tag{4.21}$$

The angular sequence for the reinjection switching sequence (repeats every $\frac{\pi}{6}$ radians) is (c.f. Fig. 4.16):

$$\beta_i = \frac{(2i-1)\pi}{48}, \text{ where } i = 1, 2, 3, 4. \tag{4.22}$$

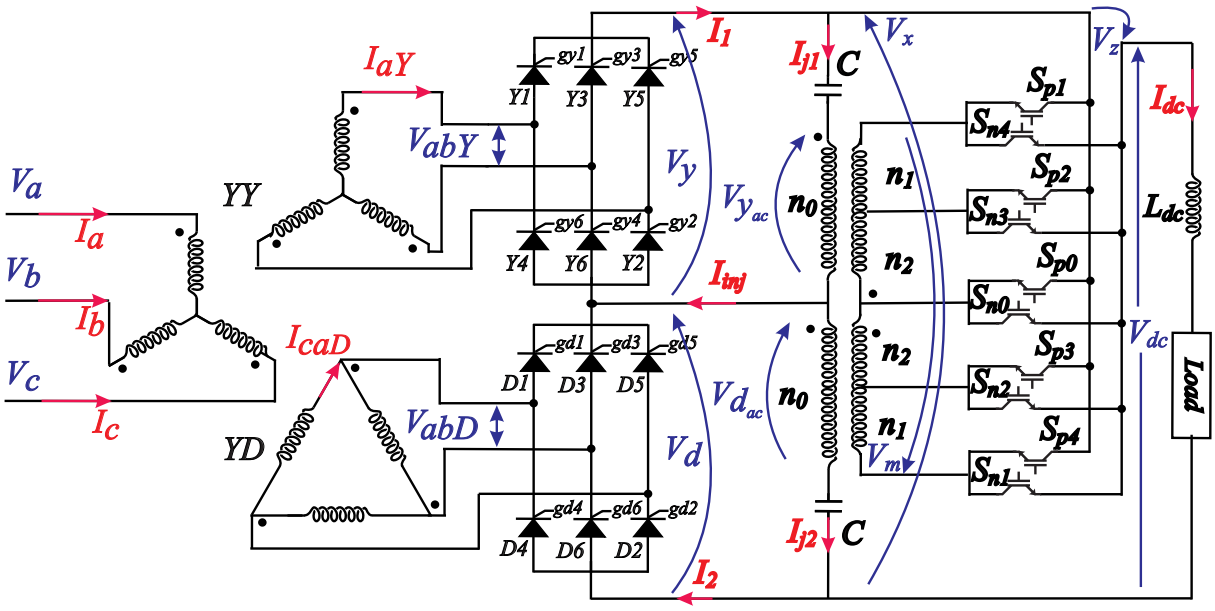


Figure 4.7: 5-level Thyristor based MLCR CSC with Linear Reinjection.

4.3.1 AC-side Current Waveforms

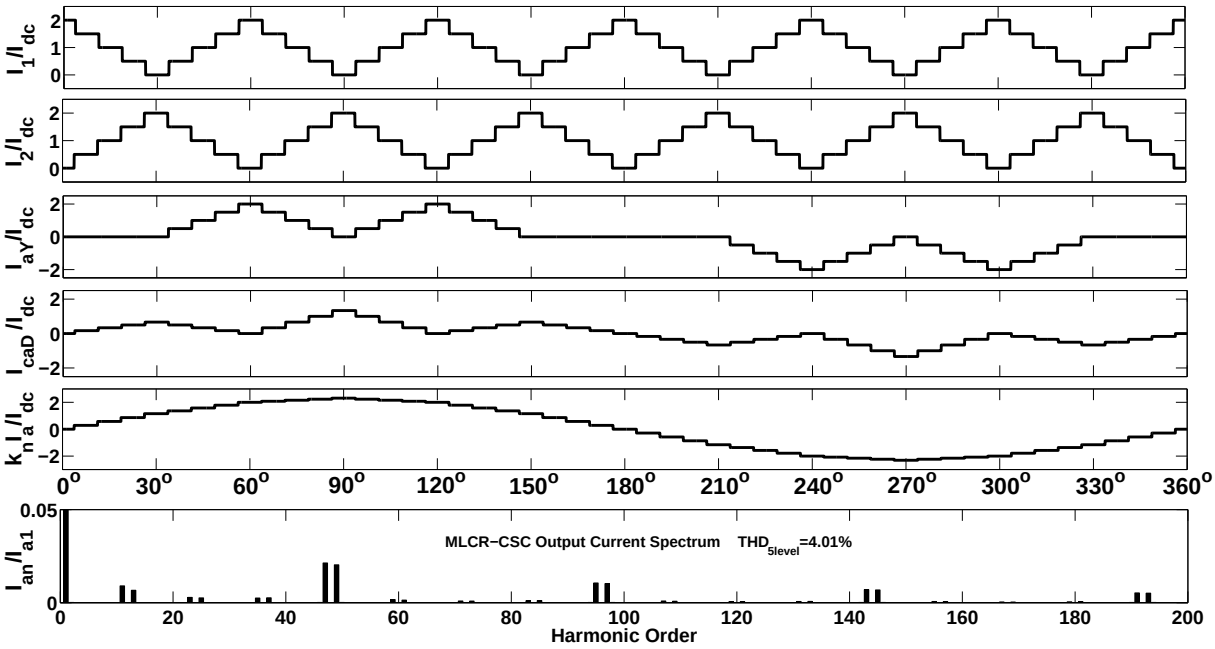


Figure 4.8: Current waveforms for a 5-level thyristor based MLCR CSC with Linear Reinjection.

Following a similar procedure to Section 4.2, the Fourier components of $I_{aY}(\omega t)$ and $I_{caD}(\omega t)$ are:

$$I_{aY_n} = \frac{2}{\pi}\int_0^{\pi} I_{aY}\sin(n\omega t)d(\omega t)$$
$$= \frac{16[1-(-1)^n]I_{dc}}{4n\pi}\sin\left(\frac{n\pi}{48}\right)\cos\left(\frac{n\pi}{6}\right)\left[4\sin\left(\frac{n\pi}{6}\right)+\sum_{i=1}^{3} i\sin\left(\frac{n\pi}{3}+\frac{n\pi}{24}\right)\right] \quad (4.23)$$

$$I_{caD_n} = \frac{2}{\pi}\int_0^{\pi} I_{caD}\sin(n\omega t)d(\omega t)$$
$$= \frac{16[1-(-1)^n]I_{dc}}{12n\pi}\sin\left(\frac{n\pi}{48}\right)\cos\left(\frac{n\pi}{6}\right)\left[4\left(\sin\frac{n\pi}{3}\right)+2\sum_{i=1}^{3} i\cos\frac{n\pi}{6}\sin\left(\frac{n\pi}{3}+\frac{in\pi}{24}\right)\right] \quad (4.24)$$

The corresponding current waveforms are shown in Fig. 4.8. The peak value I_{a1} of the fundamental component of I_a is:

$$I_{a1} = \frac{32\sqrt{3}I_{dc}}{4k_n\pi}\sin\left(\frac{\pi}{24}\right)\left[2+\sum_{i=1}^{3}\sin\left(\frac{\pi}{3}+\frac{\pi}{12}\right)\right]$$
$$\simeq \frac{2.2587}{k_n}I_{dc} \quad (4.25)$$

Similarly, RMS value of I_a is:

$$I_{arms} = \frac{1.5984}{k_n}I_{dc} \quad (4.26)$$

Using Eqns. (4.25) and (4.26), $\text{THD}_{5level} = 4.01\%$ is obtained.

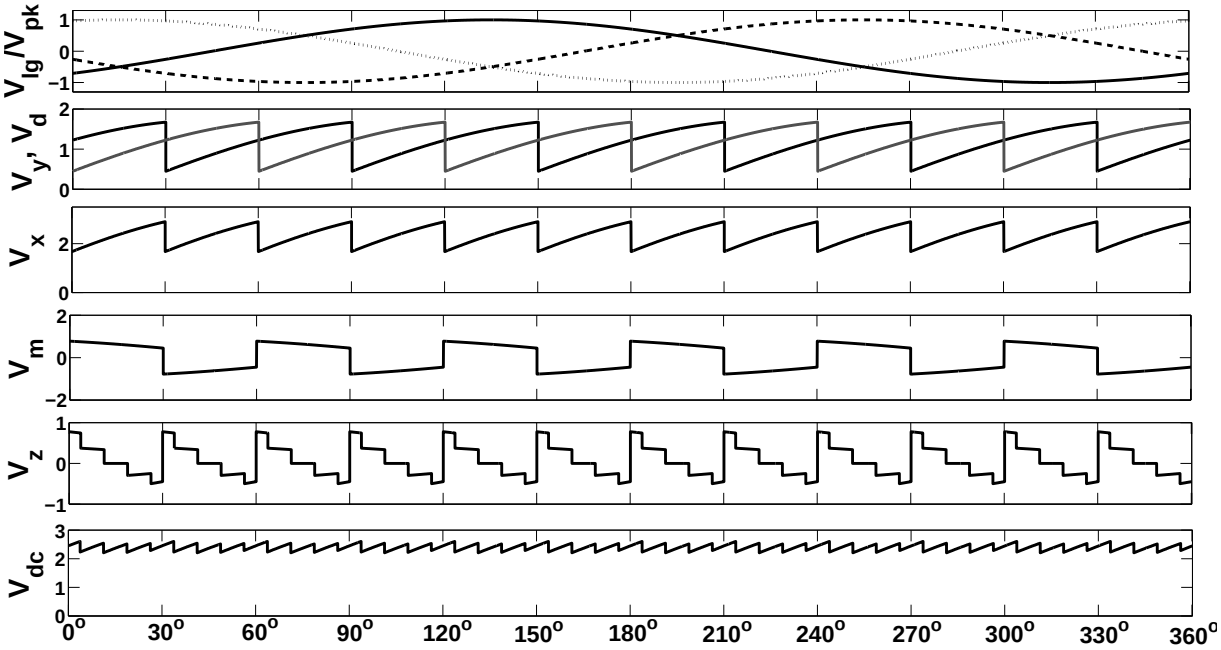


Figure 4.9: Theoretical DC voltage waveforms for a 5-level thyristor based MLCR CSC for α = -45°.

4.3.2 DC-side Voltage Waveforms

Following a similar procedure as in Section 4.2.2, the corresponding voltage waveforms are shown in Fig. 4.9. The voltage $V_z(\omega t)$ for this case is:

$$V_z(\omega t) = \begin{cases} V_m(\omega t), & 0 \leq \omega t \leq \frac{\pi}{48} \\ 0.5V_m, & \frac{\pi}{48} \leq \omega t \leq \frac{3\pi}{48} \\ 0, & \frac{3\pi}{48} \leq \omega t \leq \frac{5\pi}{48} \\ -0.5V_m, & \frac{5\pi}{48} \leq \omega t \leq \frac{7\pi}{48} \\ -V_m(\omega t), & \frac{7\pi}{48} \leq \omega t \leq \frac{9\pi}{48} \\ -0.5V_m(\omega t), & \frac{9\pi}{48} \leq \omega t \leq \frac{11\pi}{48} \\ 0, & \frac{11\pi}{48} \leq \omega t \leq \frac{13\pi}{48} \\ 0.5V_m(\omega t), & \frac{13\pi}{48} \leq \omega t \leq \frac{15\pi}{48} \\ V_m(\omega t), & \frac{15\pi}{48} \leq \omega t \leq \frac{\pi}{3} \end{cases} \tag{4.27}$$

From Fig. 4.9 it can be seen that there are 4 voltage pulses for every 30°. The average V_{dc} is:

$$V_{dc} = \frac{48\sqrt{3}V_{pk}}{4\pi k_n}\sin\left(\frac{\pi}{48}\right)\left[2+\sum_{i=1}^{3} i\sin\left(\frac{\pi}{3}+\frac{\pi}{12}\right)\right]\cos(\alpha)$$
$$\approx 3.388\frac{V_{pk}}{k_n}\cos(\alpha) \tag{4.28}$$

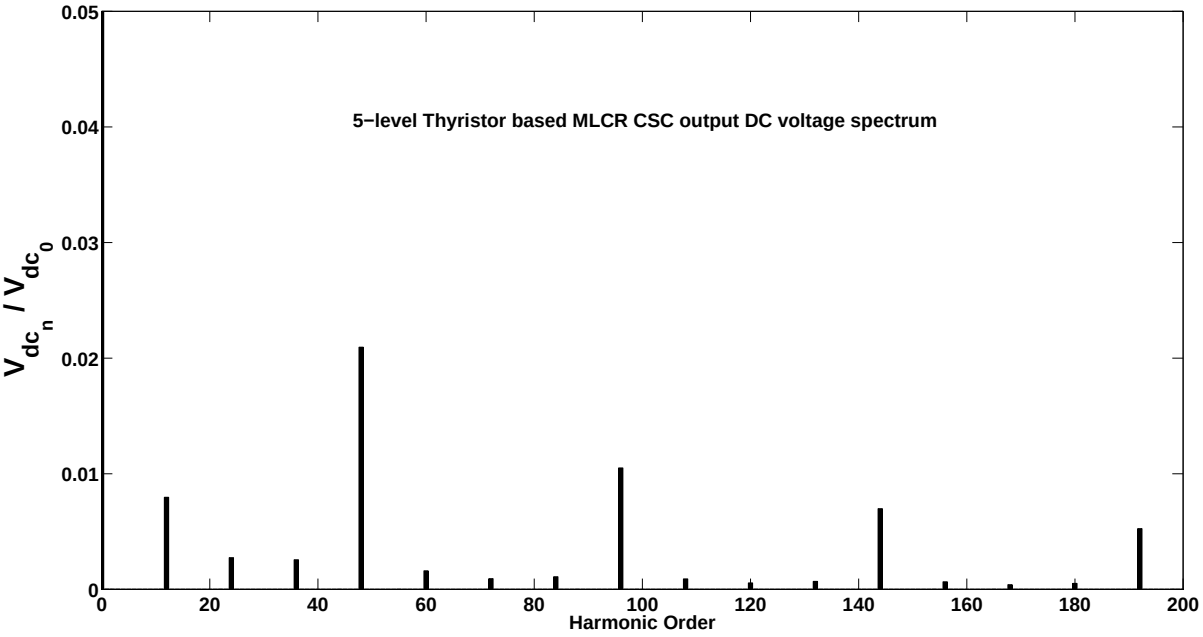


Figure 4.10: Harmonic spectrum of V_{dc} of 5-level thyristor based MLCR CSC for α = -45°.

The harmonic spectrum of V_{dc} is shown in Fig. 4.10. It can be clearly seen that a predominantly 48-pulse operation is obtained with the 48^{th} harmonic being the most dominant one. Small amount of 12-pulse related harmonics such as 12^{th}, 36^{th}, 60^{th} etc can also be seen but the magnitude is negligible.

4.4 7-LEVEL THYRISTOR BASED MLCR CSC

Fig. 4.11 shows the 7-level thyristor based MLCR CSC. The reinjection transformer used for this converter is a single-phase four-winding transformer with turns ratio (c.f. Fig. 4.11):

$$\frac{n_3}{n_0} = 0.333,\ \frac{n_2}{n_0} = 0.333 \text{ and } \frac{n_1}{n_0} = 0.333 \tag{4.29}$$

Table 4.3 shows the corresponding relationship between I_1 and I_2, I_{j1} and I_{j2} with the corresponding reinjection IGBT ON-state. The angular sequence for the reinjection switching

Table 4.3: Reinjection Switching Combinations and 7-level Reinjection Current.

On-state switches	I_{j1}	I_1	I_{j2}	I_2
Sp1/Sn1	I_{dc}	$2I_{dc}$	-I_{dc}	0
Sp2/Sn2	$0.66I_{dc}$	$1.66I_{dc}$	-$0.66I_{dc}$	$0.33I_{dc}$
Sp3/Sn3	$0.33I_{dc}$	$1.33I_{dc}$	-$0.33I_{dc}$	$0.66I_{dc}$
Sp0/Sn0	0	I_{dc}	0	I_{dc}
Sp4/Sn4	-$0.33I_{dc}$	$0.66I_{dc}$	-$0.33I_{dc}$	$1.33I_{dc}$
Sp5/Sn5	-$0.66I_{dc}$	$0.33I_{dc}$	-$0.66I_{dc}$	$1.66I_{dc}$
Sp6/Sn6	-I_{dc}	0	I_{dc}	$2I_{dc}$

sequence (repeats every $\frac{\pi}{6}$ radians) is (c.f. Fig. 4.17):

$$\beta_i = \frac{(2i-1)\pi}{72}, \quad \text{where } i = 1,\ 2,\ 3,\ 4,\ 5,\ 6. \tag{4.30}$$

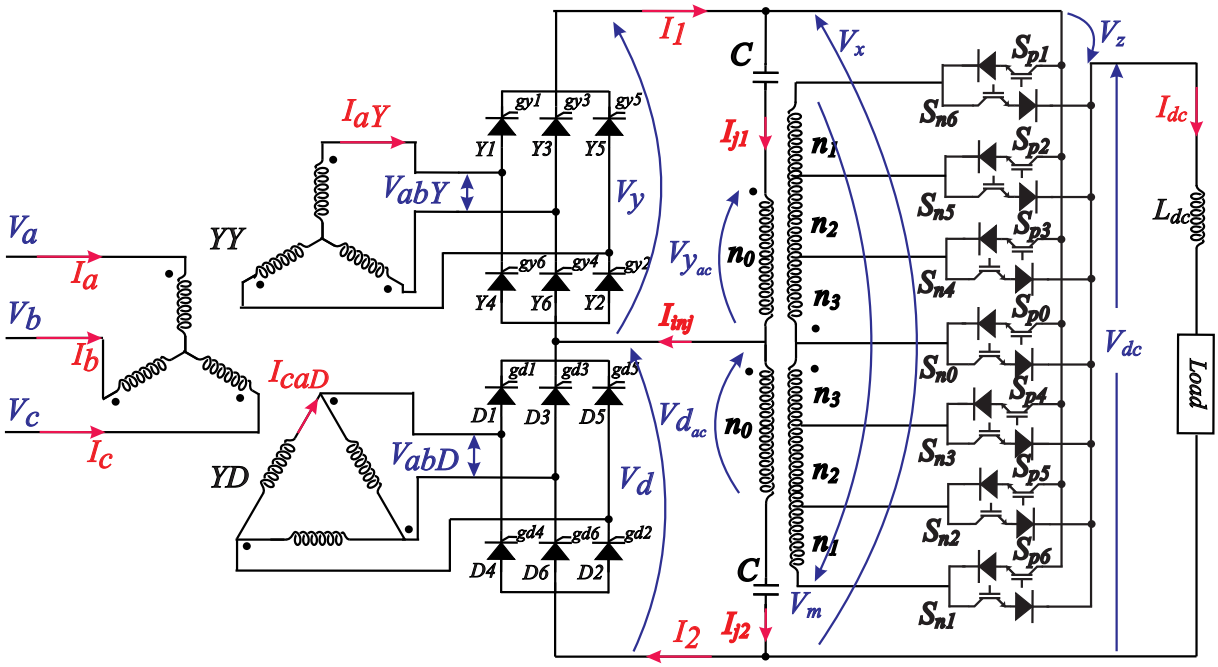


Figure 4.11: 7-level Thyristor based MLCR CSC with Linear Reinjection.

4.4.1 AC-side Current Waveforms

Again, following a similar procedure to Section 4.2, the Fourier components of $I_{aY}(\omega t)$ and $I_{caD}(\omega t)$ are:

$$I_{aY_n} = \frac{2}{\pi}\int_0^{\pi} I_{aY}\sin(n\omega t)d(\omega t)$$
$$= \frac{16[1-(-1)^n]I_{dc}}{6n\pi}\sin\left(\frac{n\pi}{72}\right)\cos\left(\frac{n\pi}{6}\right)\left[6\left(\sin\frac{n\pi}{6}\right)+\sum_{i=1}^{5} i\sin\left(\frac{n\pi}{3}+\frac{n\pi}{72}\right)\right] \quad (4.31)$$

$$I_{caD_n} = \frac{2}{\pi}\int_0^{\pi} I_{caD}\sin(n\omega t)d(\omega t)$$
$$= \frac{16[1-(-1)^n]I_{dc}}{18n\pi}\sin\left(\frac{n\pi}{72}\right)\cos\left(\frac{n\pi}{6}\right)\left[6\sin\left(\frac{n\pi}{3}\right)+2\sum_{i=1}^{5} i\cos\frac{n\pi}{6}\sin\left(\frac{n\pi}{3}+\frac{in\pi}{36}\right)\right] \quad (4.32)$$

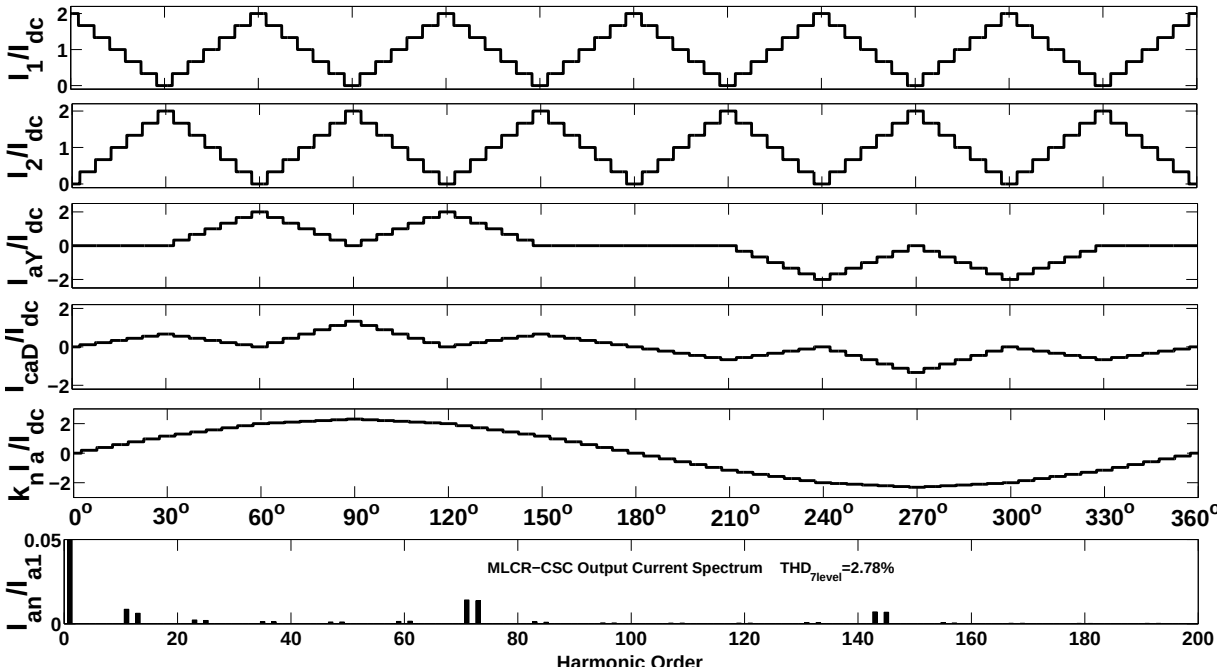


Figure 4.12: Current waveforms for a 7-level thyristor based MLCR CSC with Linear Reinjection.

The peak value (I_{a1}) of fundamental component of I_a is:

$$I_{a1} = \frac{32\sqrt{3}I_{dc}}{6\pi}\sin\left(\frac{\pi}{72}\right)\left[3+\sum_{i=1}^{5} i\sin\left(\frac{\pi}{3}+\frac{i\pi}{36}\right)\right]$$
$$\simeq \frac{2.2578}{k_n}I_{dc} \quad (4.33)$$

The RMS value of I_a is :

$$I_{arms} = \frac{1.5971}{k_n} I_{dc} \tag{4.34}$$

By using Eqns. (4.33), (4.34), $\text{THD}_{7level} = 2.78\%$.

4.4.2 DC-side Voltage Waveforms

The DC-side voltage waveforms are shown in Fig. 4.13. The voltage $V_z(\omega t)$ for a 7-level MLCR CSC is:

$$V_z(\omega t) = \begin{cases} V_m(\omega t), & 0 \leq \omega t \leq \frac{\pi}{72} \\ 0.66V_m(\omega t), & \frac{\pi}{72} \leq \omega t \leq \frac{3\pi}{72} \\ 0.33V_m(\omega t), & \frac{3\pi}{72} \leq \omega t \leq \frac{5\pi}{72} \\ 0, & \frac{5\pi}{72} \leq \omega t \leq \frac{7\pi}{72} \\ -0.33V_m(\omega t), & \frac{7\pi}{72} \leq \omega t \leq \frac{9\pi}{72} \\ -0.66V_m(\omega t), & \frac{9\pi}{72} \leq \omega t \leq \frac{11\pi}{72} \\ -V_m(\omega t), & \frac{11\pi}{72} \leq \omega t \leq \frac{13\pi}{72} \\ -0.66V_m(\omega t), & \frac{13\pi}{72} \leq \omega t \leq \frac{15\pi}{72} \\ -0.33V_m(\omega t), & \frac{15\pi}{72} \leq \omega t \leq \frac{17\pi}{72} \\ 0, & \frac{17\pi}{72} \leq \omega t \leq \frac{19\pi}{72} \\ 0.33V_m(\omega t), & \frac{19\pi}{72} \leq \omega t \leq \frac{21\pi}{72} \\ 0.66V_m(\omega t), & \frac{21\pi}{72} \leq \omega t \leq \frac{23\pi}{72} \\ V_m(\omega t), & \frac{23\pi}{72} \leq \omega t \leq \frac{24\pi}{72} \end{cases} \tag{4.35}$$

There are 6 voltage pulses for every $\frac{\pi}{6}$ radians. The average V_{dc} is:

$$\begin{aligned} V_{dc} &= \frac{48\sqrt{3}V_{pk}}{6\pi} \sin\left(\frac{\pi}{72}\right) \left[3 + \sum_{i=1}^{5} i \sin\left(\frac{\pi}{3} + \frac{i\pi}{36}\right)\right] \cos(\alpha) \\ &\approx 3.38 \frac{V_{pk}}{k_n} \cos(\alpha) \end{aligned} \tag{4.36}$$

The harmonic spectrum of V_{dc} is shown in Fig. 4.14. It can be clearly seen that a predominantly 72-pulse operation is obtained with the 72^{nd} and 144^{th} harmonic are the most dominant one.

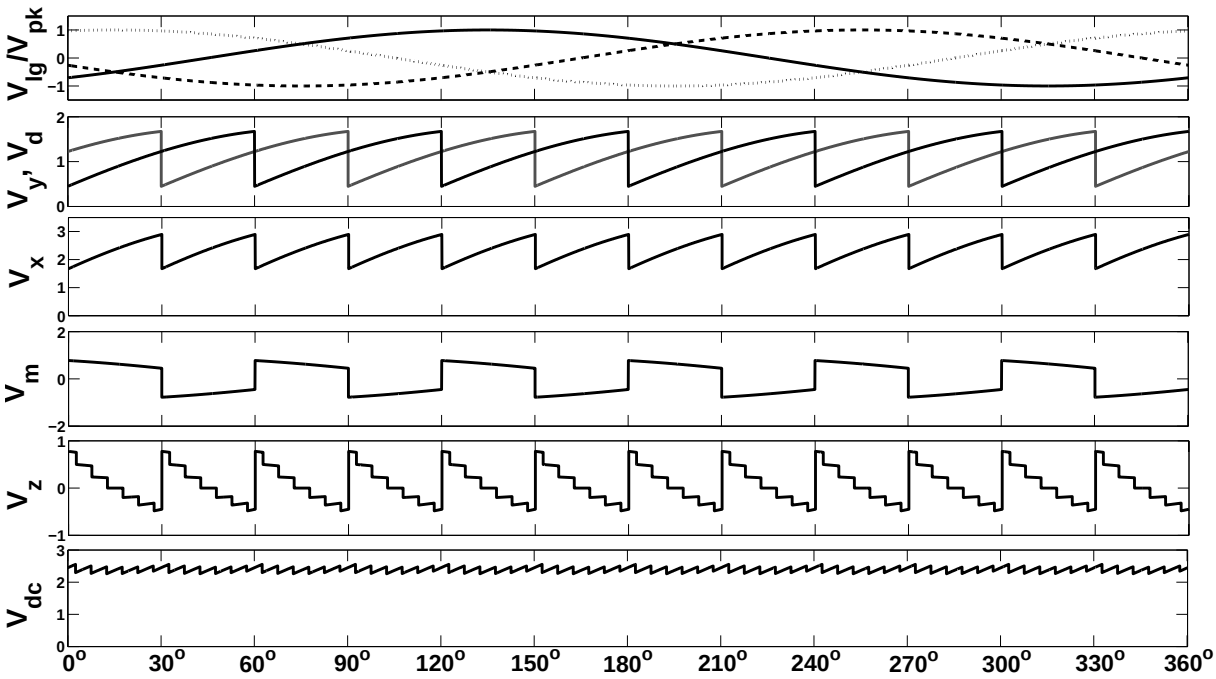


Figure 4.13: Theoretical DC voltage waveforms for a 7-level thyristor based MLCR CSC for α = -45°.

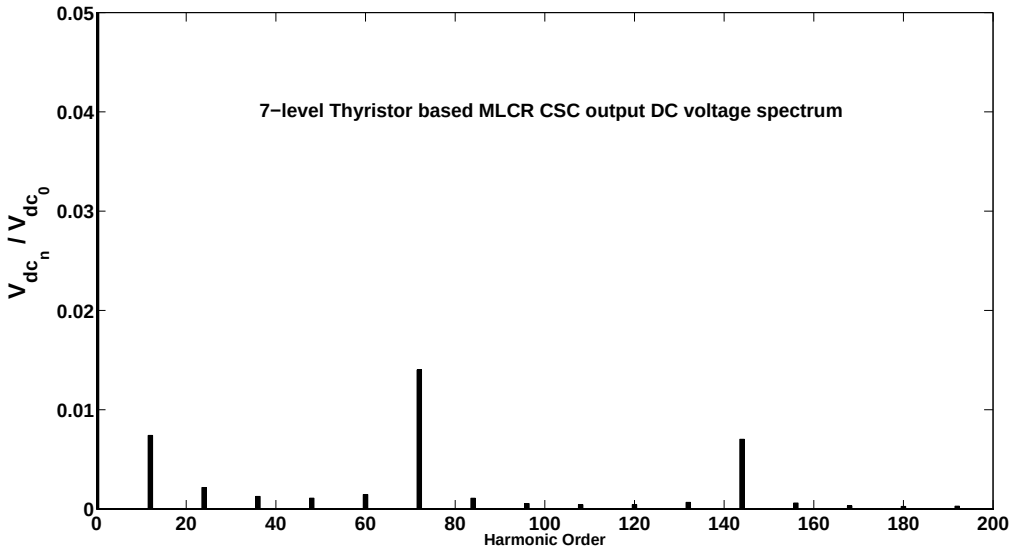


Figure 4.14: Harmonic spectrum of V_{dc} of 7-level thyristor based MLCR CSC for α = -45°.

4.5 COMPARISON BETWEEN M-LEVELS

4.5.1 Comparison based on THD

The calculated and simulated THD values are listed in Table 4.4. Based on the line current THD values obtained, the 7-level MLCR CSC provides the lowest THD.

Table 4.4: Line current THD for Linear Reinjection waveform.

Level	3	5	7
THD_{cal}	7.77%	4.01%	2.78%
THD_{sim}	7.89%	4.48%	3.13%

It is obvious that a higher level results in less harmonic content on the AC-side line currents. Also, due to the step-by-step varying I_1 and I_2, the higher level used will induce less $\frac{dV}{dt}$ stress on the main bridge switches.

4.5.2 Comparison based on Turns Ratio of the Reinjection Transformer

The reinjection transformer operates at six times the fundamental frequency. It is clearly inferred from Sections 4.2 - 4.3 that as level number m increases, custom made reinjection transformers with turns ratio which are difficult to achieve are needed. Hence, for practical purposes, reinjection transformers up to 7-level MLCR CSC are feasible. However, the main limitation for 7-level high power MLCR CSC will be due to the unavailability of high power thyristors with fast reverse recovery time.

4.5.3 Comparison based on Complexity of the Reinjection Control Circuit

In order to produce the firing sequence needed to generate a variable DC bus currents I_1 and I_2, the firing sequence of the reinjection switches are synchronised with the main thyristor bridge switching. As the main bridge thyristors can be forced off, the firing angles can be either positive or negative as commutation is independent of the line voltage. For a 3-level MLCR CSC, the firing pattern is shown in Fig. 4.15. The outermost circle representing the reinjection switch firing sequence is divided into 24 sectors. The 12 zero current intervals of the 3-level reinjection scheme are switched ON for 15° while the remaining sectors are also switched ON for 15° to maintain equal width criterion.

For a 5-level MLCR CSC, the firing pattern is shown in Fig. 4.16 with 48 sectors in the outermost circle. Here, the reinjection switches are ON for a period of 7.5°. Similarly, Fig. 4.17 shows the firing sequence for a 7-level MLCR CSC. Here, the zero current duration during main bridge commutation regions is set at 5°. The following zero current intervals are maintained in the three cases:

- 3-level MLCR CSC: 833.34 μs.
- 5-level MLCR CSC: 416.67 μs.

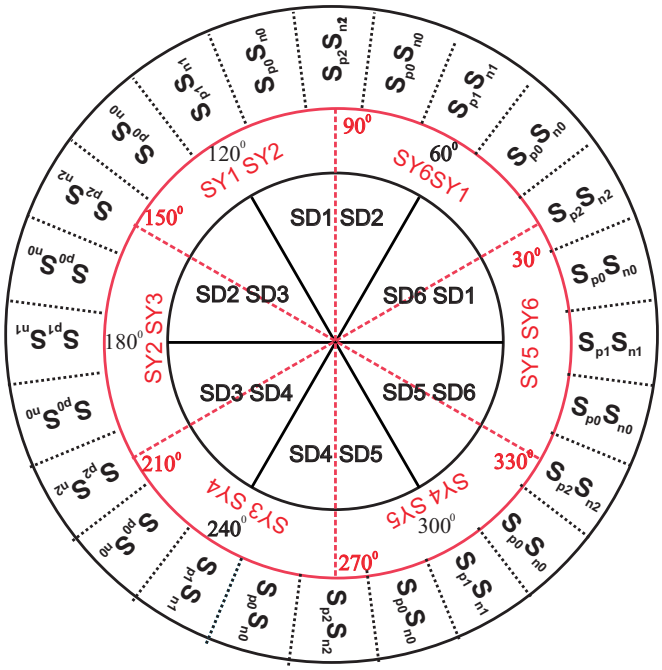


Figure 4.15: Firing pattern for 3-level MLCR CSC.

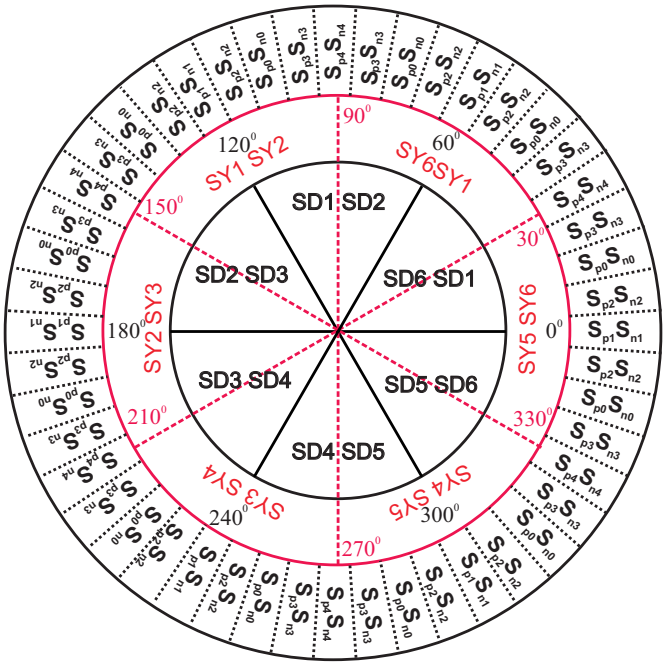


Figure 4.16: Firing pattern for 5-level MLCR CSC.

- 7-level MLCR CSC: 277.78 μs.

These durations provide enough time for the thyristor to regain its blocking capability for different m-levels. But the complexity of the switching pattern increases with the increase in the level number.

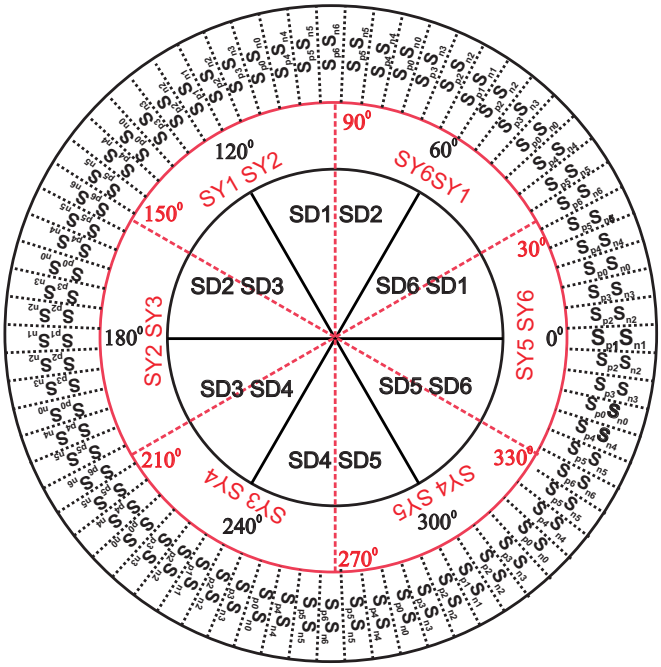


Figure 4.17: Firing pattern for 7-level MLCR CSC.

4.5.4 Comparison based on Reinjection Switch Ratings

Voltage ratings

The maximum voltage that a reinjection switch is subjected to is when $V_z(\omega t) = V_m(\omega t) = [V_y(\omega t) - V_d(\omega t)]$. Hence, the maximum voltage rating of the reinjection switch (for any level) is:

$$V_{Spi/Sni} = 2\sqrt{3}\frac{V_{pk}}{k_n}\sin\left(\frac{\pi}{12}\right) \tag{4.37}$$

The voltage rating of the main bridge thyristor is:

$$V_{thy_i} = \sqrt{3}\frac{V_{pk}}{k_n} \tag{4.38}$$

From (4.37) and (4.38) it can be deduced that:

$$V_{Spi/Sni} = 0.5176V_{thy_i} \tag{4.39}$$

Current ratings

The RMS current rating of the Y-connected secondary-side is:

$$I_{aY_{rms}} = \frac{2\sqrt{2+(m-1)^{-2}}}{3} I_{dc} \tag{4.40}$$

The RMS current rating of the main bridge thyristor is:

$$I_{T_{rms}} = \frac{I_{aY_{rms}}}{\sqrt{2}} \tag{4.41}$$

In the Figs. 4.18 - 4.19, the various current waveforms in the reinjection circuit for a 3-level MLCR CSC are shown. The 'chopping' of load current I_{dc} occurs with the help of the reinjection IGBTs.

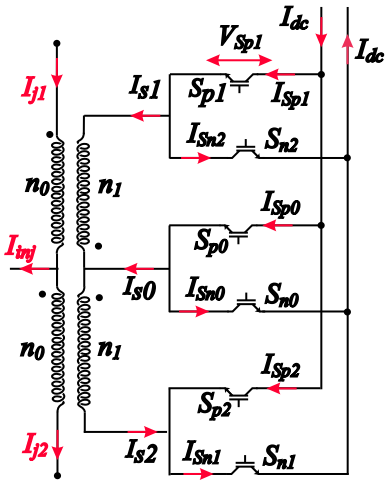
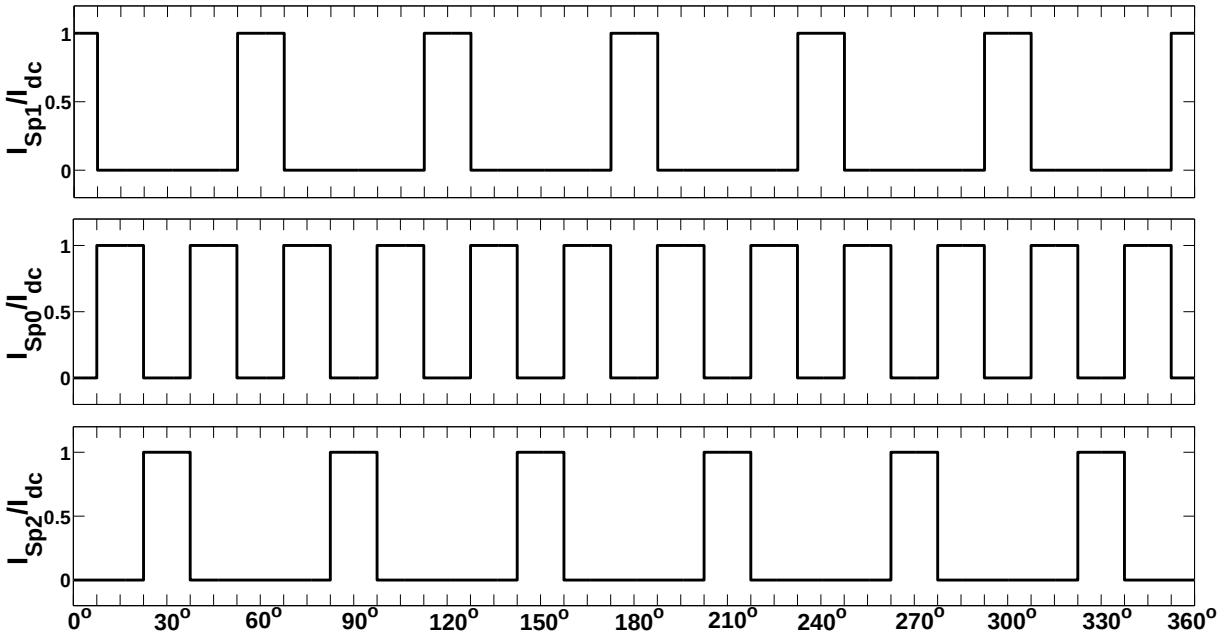


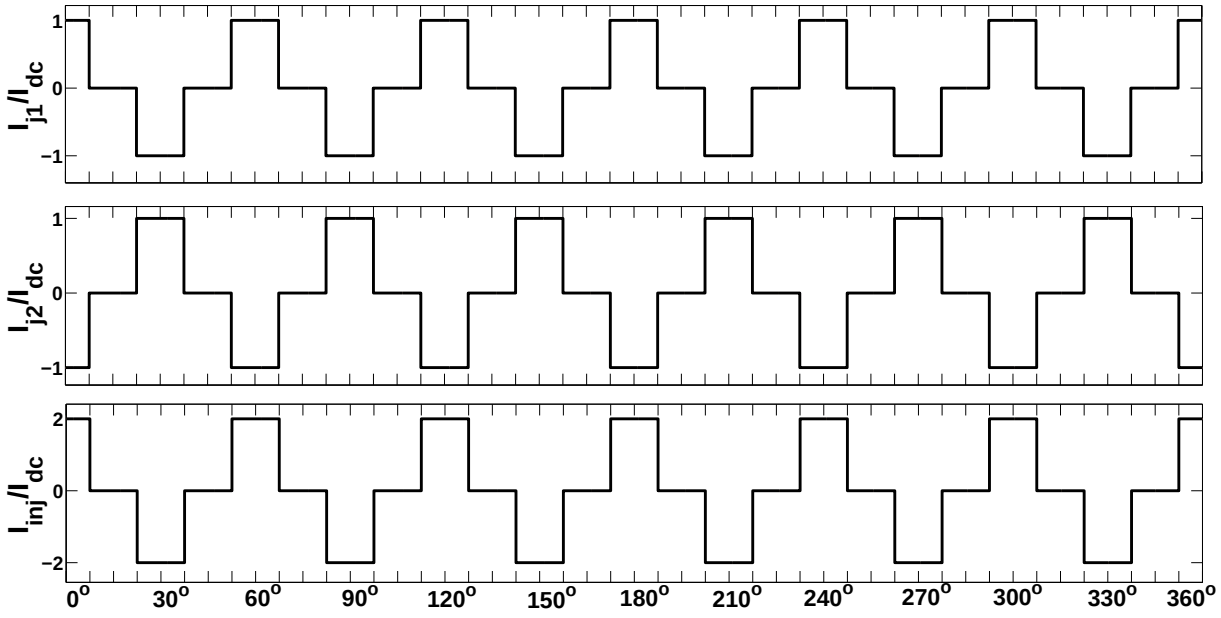
Figure 4.18: Reinjection current flow for a 3-level MLCR CSC.

The DC currents flowing through S_{p1}, S_{p0} and S_{p2} are shown in Fig. 4.19(a). The different IGBT switching pairs form the reinjection transformer secondary-side currents I_{s1}, I_{s0} and I_{s2} which are reflected to the primary-side to form I_{j1} and I_{j2}. The reinjection current I_{inj} is shown in 4.19(b).

The RMS current rating of reinjection switch pairs (Sp1/Sn1) and (Sp2/Sn2) is calculated from Fig. 4.19(b). In the case of a symmetrical waveform it is acceptable to choose the duration from 0° through 30°.



(a): I_{Sp1}, I_{Sp0} and I_{Sp2} waveforms



(b): I_{j1}, I_{j2} and I_{inj} waveforms

Figure 4.19: Theoretical waveforms in the reinjection circuit.

$$I_{rms} = \sqrt{\frac{1}{\pi/6}\int_{0}^{\pi/24} I_{dc}^2 \cdot d\theta}$$
$$= 0.5 \times I_{dc} \tag{4.42}$$

Similarly, RMS current rating of reinjection switch pairs (Sp0/Sn0) is calculated as:

$$I_{rms} = \sqrt{\frac{1}{\pi/6}\int_{\pi/24}^{\pi/8} I_{dc}^2 \cdot d\theta}$$
$$= 0.707 \times I_{dc} \tag{4.43}$$

The reinjection switch current ratings for 3-level MLCR CSC are:

- From Eqn. 4.41 the main bridge thyristors have a RMS current rating of $0.707I_{dc}$.
- Reinjection switch pairs (Sp1/Sn1) and (Sp2/Sn2) have a RMS current rating of $0.5I_{dc}$.
- Reinjection switch pair (Sp0/Sn0) have a RMS current rating of $0.707I_{dc}$.

Hence it can be found that reinjection switch pairs (Sp1/Sn1) and (Sp2/Sn2) have a RMS current rating 0.707 times that of main bridge thyristors and the corresponding rating for (Sp0/Sn0) is I_{dc}.

The reinjection switch current ratings for 5-level MLCR CSC are:

- From Eqn. 4.41 the main bridge thyristors have a RMS current rating of $0.677I_{dc}$.
- Reinjection switch pairs (Sp1/Sn1) and (Sp4/Sn4) have a RMS current rating of $0.3535I_{dc}$.
- Reinjection switch pairs (Sp0/Sn0), (Sp2/Sn2) and (S3/Sn3) have a RMS current rating of $0.5I_{dc}$.

Similarly, it can be found that reinjection switch pairs (Sp1/Sn1) and (Sp4/Sn4) have a RMS current rating 0.5222 times that of main bridge thyristors and the corresponding rating for all remaining switch pairs is 0.7385.

The reinjection switch current ratings for a 7-level MLCR CSC are:

- From Eqn. 4.41 the main bridge thyristors have a RMS current rating of $0.671I_{dc}$.

- Reinjection switch pairs (Sp1/Sn1) and (Sp6/Sn6) have a RMS current rating of $0.288I_{dc}$.
- Reinjection switch pairs (Sp0/Sn0),(Sp2/Sn2), (Sp3/Sn3), (Sp4/Sn4) and (Sp5/Sn5) have a RMS current rating of $0.4082I_{dc}$.

Similarly, it can be found that reinjection switch pairs (Sp1/Sn1) and (Sp6/Sn6) have a RMS current rating 0.4294 times that of main bridge thyristors and the corresponding rating for all remaining switch pairs is 0.6083.

Although the ratings of the reinjection switches reduce as m-level increases, other factors like reinjection transformer turns ratio, switching complexity etc limit the practical application of higher m-levels.

4.6 DC BLOCKING CAPACITORS FOR 3-LEVEL MLCR CSC

This section presents the effect in the choice of the DC blocking capacitor which was not included in the theoretical derivations. In general, the DC blocking capacitor (C) should behave like a short at the operating frequency and the impedance offered at the operating frequency should be as low as possible. The repetition frequency of the reinjection current and voltage waveforms is 300 Hz. The impedance (X_c) is calculated as $X_c = \frac{1}{2\pi fC}$ and different values of X_c for different DC blocking capacitors is presented in Table 4.5.

Table 4.5: Capacitor Impedance variation with different DC blocking capacitor.

C	X_c
50 μF	10.61 Ω
100 μF	5.305 Ω
500 μF	1.061 Ω
1 mF	0.5305 Ω
2 mF	0.2652 Ω

Fig. 4.20 shows the transient time taken to reach steady-state voltage across C (V_c) and the ripple voltage (V_{ripple}) for different values of C. V_{ripple} across C is inversely proportional to its capacitance value and a trade-off is required between transient time and V_{ripple}. A lower value of V_{ripple} requires a higher value of C, and will make V_m closer to its theoretical value. In Section 4.2.2, $V_m(\omega t)$ was derived under the assumption that V_{ripple} across the capacitor was negligible. But for a practical value of capacitance, there resulting ripple voltage modifies $V_m(\omega t)$ as:

$$V_m(\omega t) = [V_y(\omega t) - V_d(\omega t) - 2V_{ripple}(\omega t)] \tag{4.44}$$

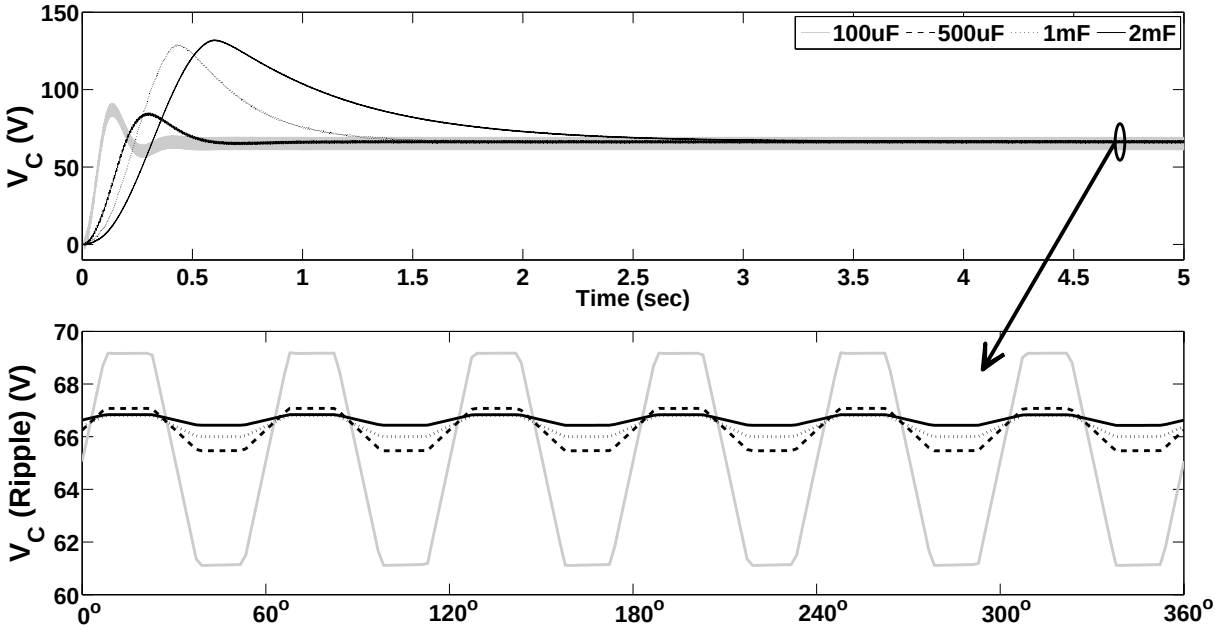


Figure 4.20: V_c transient characteristics with V_{ripple} for different DC blocking capacitors.

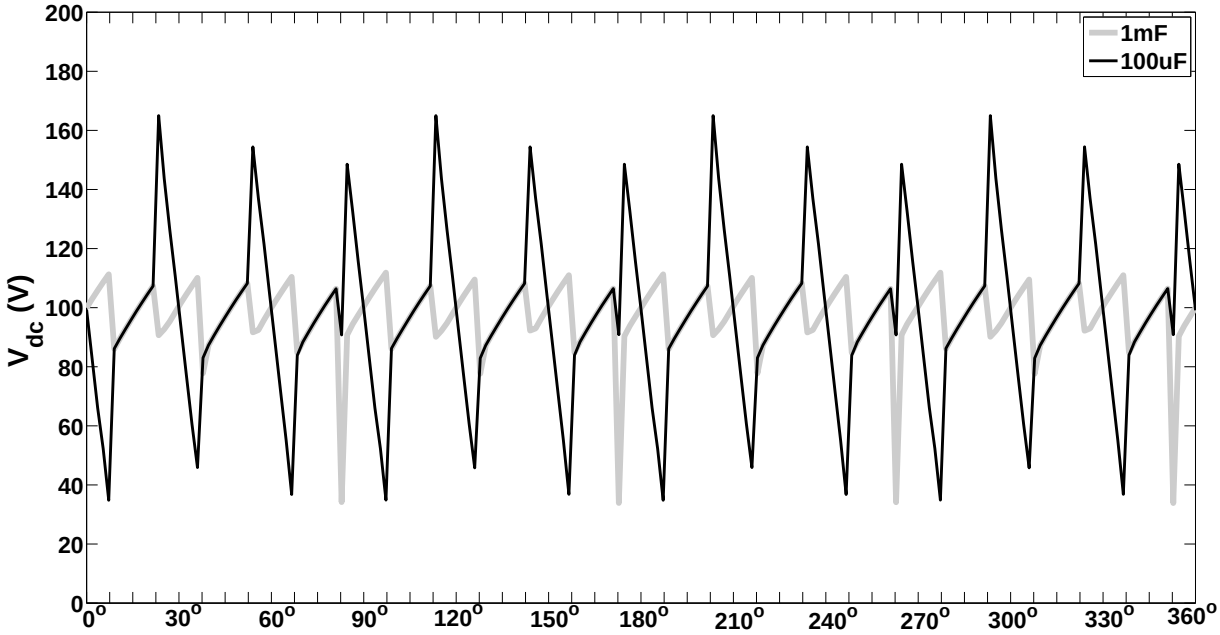


Figure 4.21: Effect of V_{ripple} on V_{dc} characteristics.

The variation in V_{dc} from its theoretical value for two different DC blocking capacitor values is shown in Fig. 4.21. As can be clearly seen $X_c \leq 5\ \Omega$, i.e a DC blocking capacitor C $\geq 100\ \mu F$ is needed to maintain 24-pulse characteristics for a 3-level MLCR CSC. When $X_c \leq 5\ \Omega$ the 24^{th} harmonic in V_{dc} is the most dominant one whereas when $X_c \geq 5\ \Omega$, the 12^{th} harmonic increases. As $V_m(\omega t)$ is modified, V_{dc} is also modified from its theoretical shape and the harmonic spectrum of V_{dc} is influenced by V_{ripple}. Based on the above simulation, a DC blocking capacitor C = 1 mF is chosen as a good trade-off.

4.7 CHOICE OF SNUBBER CIRCUITS FOR 3-LEVEL MLCR CSC

A simulation study, using PSCAD/EMTDC, is carried out to study the influence of an RCD snubber across the reinjection switches on the performance of a 3-level thyristor based MLCR CSC. An RCD snubber circuit is necessary across the reinjection switches to limit the sharp rise in voltage across it due to the sudden interruption of current flowing through it.

4.7.1 Waveforms without RCD snubber

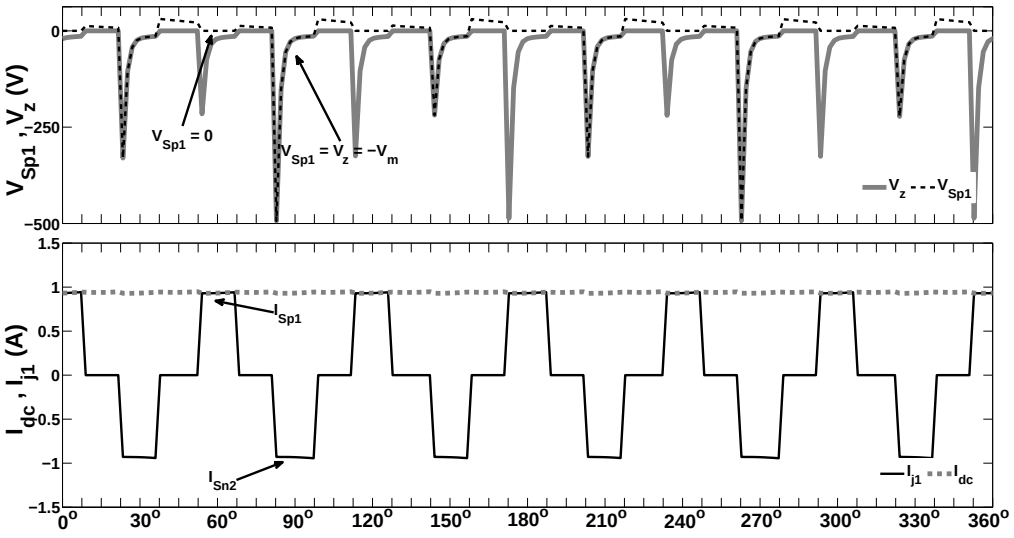


Figure 4.22: V_{Sp1} and I_{S1} with no snubber.

The voltage waveform across the reinjection IGBT $Sp1$ (V_{Sp1}) and the reinjection current (I_{j1}) flowing in the primary-side of reinjection transformer, without an RCD snubber, is shown in Fig. 4.22. It can be clearly seen that there is a sharp rise in voltage across V_{Sp1} whenever there is a current transition through it (e.g. current transition from 0 to -I_{dc} or 0 to I_{dc}). This effect was not considered while deriving the theoretical waveforms. As seen from Fig. 4.23, these voltage spikes occur across the individual DC voltage waveform of the two 6-pulse bridges which in turn

affect the voltages V_m and V_z. The spikes occur exactly 7.5° before and after the theoretical main bridge switching instant. Thus, there is a need to limit the voltage spikes using an RCD snubber to a safe operating level so that the voltage across the main bridge switches, voltage across reinjection switches, DC blocking capacitor and the reinjection transformer is below their rated values. The simulated AC-side current waveforms are shown in Fig. 4.24. The line current THD = 7.8% is very close to the calculated theoretical value.

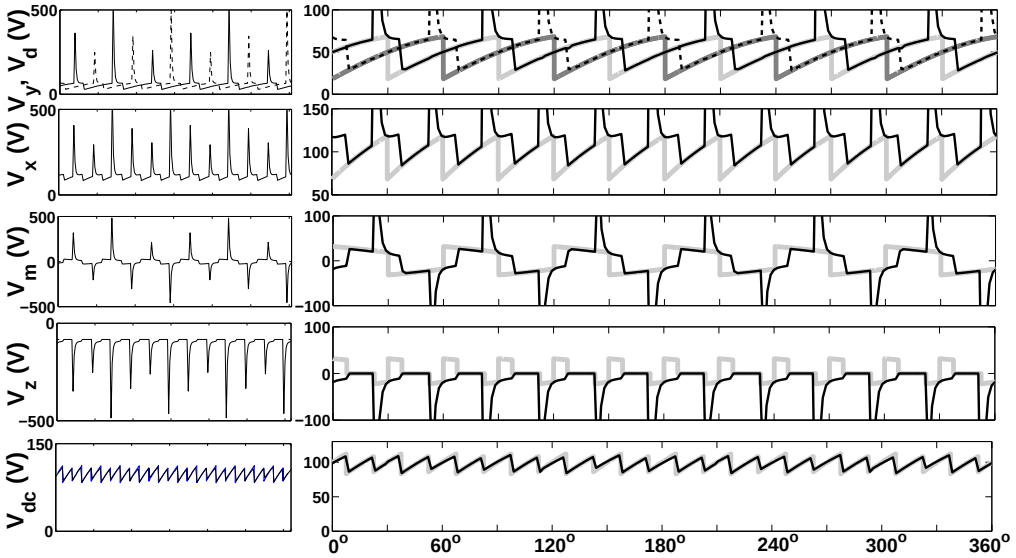


Figure 4.23: Simulated DC voltage waveforms for a 3-level thyristor based MLCR CSC for α = -45° without an RCD snubber.

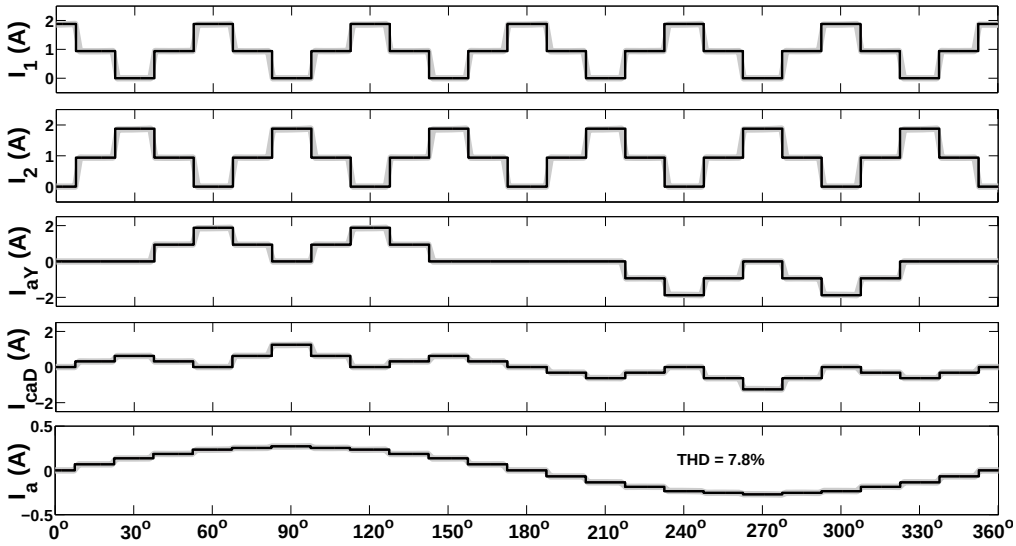
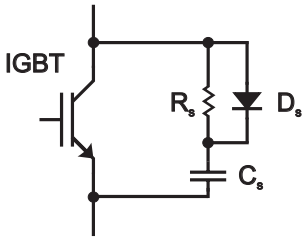
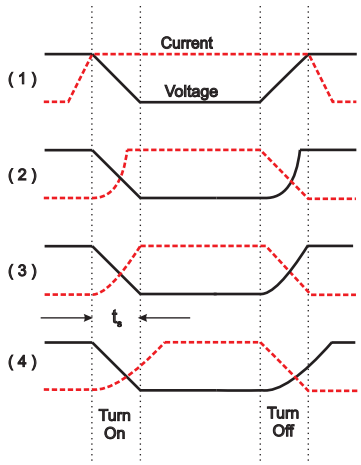


Figure 4.24: Simulated AC current waveforms for a 3-level thyristor based MLCR CSC for α = -45° without an RCD snubber.



(a): RCD snubber for reinjection IGBT.



(b): Voltage and Current Waveforms for (1) Ideal (2) Small Snubber (3) Normal Snubber (4) Large Snubber.

Figure 4.25: Snubber consideration for Reinjection Switches.

4.7.2 Waveforms with RCD snubbers

A snubber circuit (Fig. 4.25(a)) is used to clamp the voltage spike or damp the ringing across a switch. The voltage spikes are a function of the leakage inductance in the reinjection transformer. Also the stray inductance in the circuit will include the inductance distributed over the entire circuit in the actual hardware set-up. While the snubber components are calculated assuming their effective values, there is no way to physically measure them in the circuit to achieve ideal conditions.

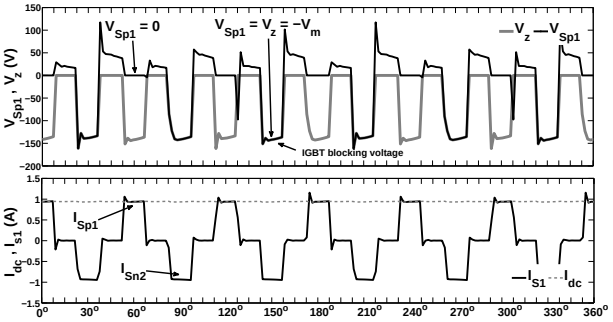
The snubber capacitor value is a trade-off as shown in Fig. 4.25(b). A 'normal' snubber is defined as the one which allows the current to reach the rated level at the same time the voltage reaches zero. A 'small' snubber allows the current to rise faster while a 'large' snubber slows the current rise rate. However, larger capacitor will provide over-clamping. When the RCD snubber is used to control the rate of voltage rise at the IGBT, the capacitor must be completely charged and discharged during each cycle to be able to control the rate-of-rise of the drain voltage. The RC time constant (τ_{RC}) of the snubber should be much smaller than the switching period. Usually, τ_{RC} should be $\frac{1}{10}^{th}$ of the switching period. The value of snubber C_{sn} is given by equation [McMurray 1980]:

$$C_{sn} = \frac{It_s}{2E} \tag{4.45}$$

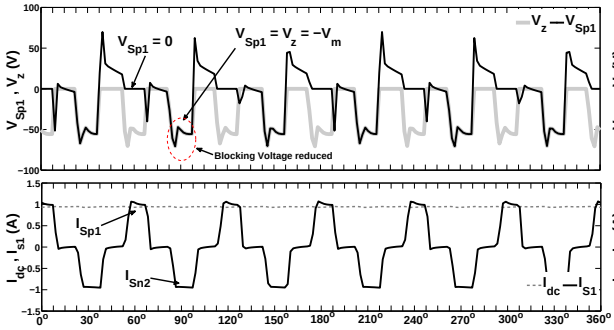
where I: maximum IGBT current (assumed) = 2 A, $t_s :\approx 1.65\ \mu$s (3 times the value given in the datasheet of the IGBT), E: the maximum expected voltage across IGBT: $\approx 0.9\frac{V_{pk}}{k_n} \approx 36.72\ V$ for the present application. Substituting these values in (4.45) gives $C_{sn} = 0.045\ \mu$F. Assuming

$C_{sn} = 0.05$ μF, the value of R_{sn} is chosen to allow (τ_{RC}) to be less than 166.66 μs ($\frac{1}{10}^{th}$ of 600 Hz, switching frequency of $Sp0/Sn0$). The selected value of $R_{sn} = 1$ kΩ which gives $(\tau_{RC}) = 50$ μs.

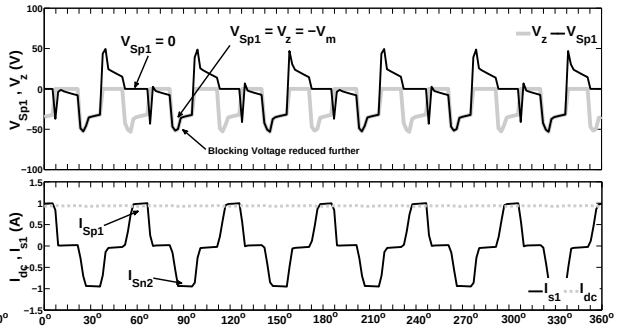
Three different cases are considered in this study, 'small' $C_{sn} = 0.01$ μF, 'large' $C_{sn} = 0.1$ μF, 'very large' $C_{sn} = 1$ μF and the results are presented in Figs. 4.26 - 4.28. From Fig. 4.26(c) the voltage across V_{sp1} is closest to its calculated value however the current rise is slow. Whereas in Fig. 4.26(a) a low value of C_{sn} provides quick rise in the current and the current resembles the theoretical current more closely. AC-side line current I_a THD = 7.9%, 8.1% and 8.7% respectively for $C_{sn} = 0.01$ μF, 0.1 μF and 1 μF (Fig. 4.27 - Fig. 4.28). The effectiveness of the MLCR scheme depends on the modification of the constant DC bus current into a quasi-triangular DC bus current using current reinjection. The use of 'small' C_{sn} is found to be the best even though the it requires over-rated reinjection IGBT switches as shown in Fig. 4.26.



(a): V_{Sp1} and I_{S1} with $C_{sn} = 0.01$ μF



(b): V_{Sp1} and I_{S1} with $C_{sn} = 0.1$ μF



(c): V_{Sp1} and I_{S1} with $C_{sn} = 1$ μF

Figure 4.26: Voltage across reinjection IGBT S_{p1} for different snubber capacitor.

4.8 CONCLUSIONS

- This chapter provided a detailed comparative study of m-level thyristor based MLCR CSC. The higher m-level MLCR CSC has definite advantages in terms of lower THD obtained, smaller reinjection switch ratings. The disadvantages of higher m-level MLCR CSC include the reinjection transformer turns ratio being difficult to achieve practically

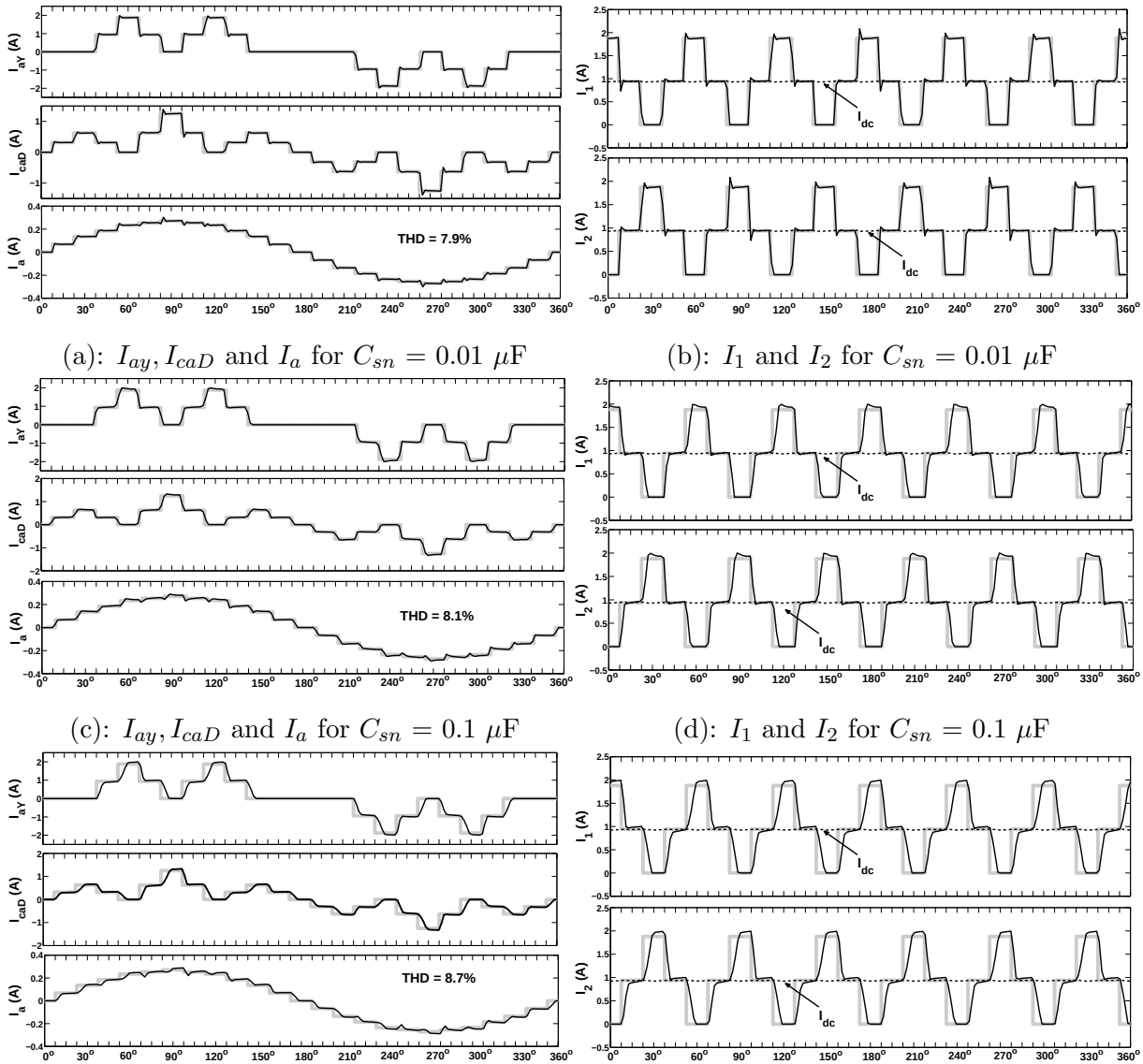
and a complex switching strategy. Diminishing returns occurs in progression to higher m-levels. A trade-off based on line current THD and reinjection transformer turns ratio is required.

- The trade-off in the choice of DC blocking capacitor was illustrated. This trade-off is between the time taken to reach steady-state and the amount of voltage ripple appearing across the DC blocking capacitor. Lower order harmonics starts to dominate in V_{dc} if a very small value of DC blocking capacitor is used and the 12(m-1) pulse characteristic of DC-side output voltage is lost.

- Three different RCD snubbers classified as 'small', moderately 'large' and 'very large' are used in a simulation to study the effect of the RCD snubbers on the performance of the 3-level MLCR CSC. The use of a 'small' snubber at the cost of using higher-rated reinjection IGBTs is again a good trade-off between higher rated reinjection switches vs quality of AC-side line current and DC-side voltage obtained.

As the thyristor based MLCR CSC has been simulated extensively using PSCAD/EMTDC, a conclusive proof of this concept requires the construction of a small-scale prototype. The prototype is to test the validity of thyristor based MLCR CSC. It is important to verify that neglecting some of the real-world artifacts (stray capacitance or inductance etc) will not imped the operation of a practical thyristor based MLCR CSC.

For this proof of concept, the relatively simple 3-level MLCR CSC is chosen. Although the performance of the 3-level MLCR CSC is not as good as the 5-level or the 7-level, it is sufficient to verify the concept.



(a): I_{ay}, I_{caD} and I_a for $C_{sn} = 0.01$ μF

(b): I_1 and I_2 for $C_{sn} = 0.01$ μF

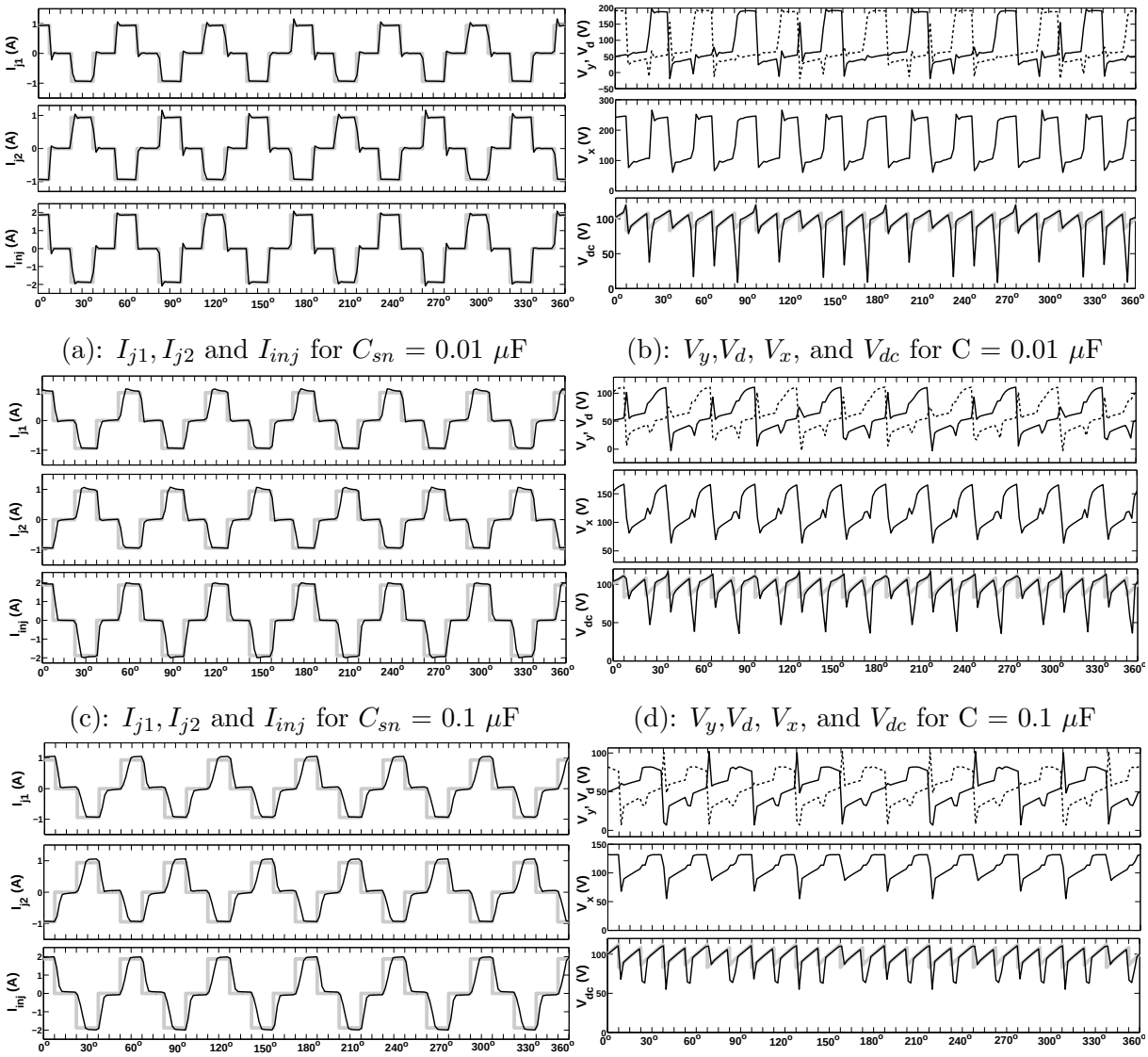
(c): I_{ay}, I_{caD} and I_a for $C_{sn} = 0.1$ μF

(d): I_1 and I_2 for $C_{sn} = 0.1$ μF

(e): I_{ay}, I_{caD} and I_a for $C_{sn} = 1$ μF

(f): I_1 and I_2 for $C_{sn} = 1$ μF

Figure 4.27: Simulated AC-side current and DC bus current waveforms for the 3-level thyristor based MLCR CSC.



(a): I_{j1}, I_{j2} and I_{inj} for $C_{sn} = 0.01$ μF

(b): V_y,V_d, V_x, and V_{dc} for C = 0.01 μF

(c): I_{j1}, I_{j2} and I_{inj} for $C_{sn} = 0.1$ μF

(d): V_y,V_d, V_x, and V_{dc} for C = 0.1 μF

(e): I_{j1}, I_{j2} and I_{inj} for $C_{sn} = 1$ μF

(f): V_y,V_d, V_x, and V_{dc} for C = 1 μF

Figure 4.28: Simulated Reinjection current and DC-side voltage waveforms for the 3-level thyristor based MLCR CSC.

Chapter 5

HARDWARE IMPLEMENTATION

5.1 INTRODUCTION

The main objective of this chapter is to present the design and development of the power and control electronics for the 3-level MLCR CSC prototype system. In particular a description is given of:

1. the driver circuit for the thyristor based converter, its implementation details and 12-pulse thyristor converter experimental results.

2. the driver circuit for the IGBT based reinjection switches and its implementation details.

3. the generation of reinjection pulses for a 3-level MLCR CSC.

4. the testing of the reinjection transformer and the determination of its various parameters.

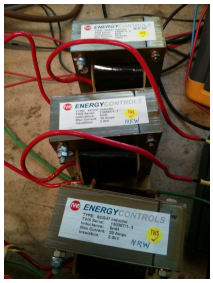
The system ratings are presented in section 5.2. Hardware details include: the generation of firing pulses having a range of $-180° \leq \alpha \leq 180°$ using TCA785 phase controller, a new forward converter based thyristor firing circuit, the opto-coupler based IGBT driver circuit, heat sink calculations, reinjection pulse generation circuits, reinjection transformer test results, etc.

5.2 SYSTEM RATINGS

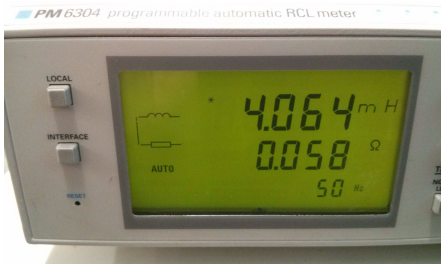
The laboratory system ratings are listed in Table 5.1, with the measured values shown in Fig. 5.1.

Table 5.1: Laboratory Parameter Ratings.

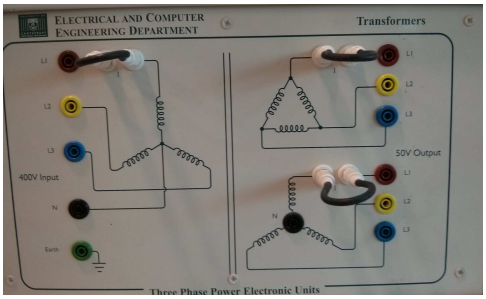
Parameter		Value
Source Specification	Voltage rating	400 V @ 50 Hz
	Impedance	0.06 Ω + 4 mH
Interface transformer	Type	3-phase, 3-winding @ 50 Hz
	Voltage rating	400 V : 50 V
Reinjection transformer	Type	1-phase, 2-winding @ 300 Hz
	Power rating	1 kVA
	Voltage rating	400 V : 400 V
Load specification	Load resistance	100 Ω
	Load inductance	500 mH



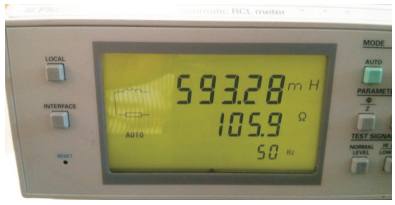
(a): Line inductor SCG47 (5 mH)



(b): Measured value of SCG47 at 50 Hz



(c): 12-pulse $Y - Y - D_{11}$ transformer



(d): Measured value of R-L load

Figure 5.1: AC-side inductor, interface transformer and the measured RL load used in the prototype.

5.2.1 Interface Transformer Ratings

For a 3-level MLCR CSC, using Eqn. 4.20, the maximum V_{dc} is:

$$V_{dc} \approx 3.39\frac{V_{pk}}{k_n}\cos(\alpha) \approx 3.39\frac{326}{8}\cos(0^\circ) \approx 138V$$

Using a load resistance, $R_{dc} \approx 100\ \Omega$, $I_{dc} \approx 1.4$ A is obtained. The no-load DC voltage calculated as (including losses):

$$V_{no-load} = (V_{dc} + 2 \times V_{th} + V_l) \times (1 + \Delta V_{trans})(1 + \Delta V_{mains}) \approx 152V \tag{5.1}$$

where:

- On-state maximum voltage drop (V_{th}) = 1.75 V (for BT152800R thyristor)
- Assuming voltage drop on due to line inductance and inner connections (V_l) = 0.5 V
- Voltage drop on transformer (ΔV_{trans}) : 2% (assumption)
- Worst case mains voltage variation (ΔV_{mains}): 5% (assumption)

For 3-level MLCR-CSC, I_s and $V_{ln_{pk}}$ in terms of I_{dc} and V_{dc} is given by:

$$I_s = \frac{1.6054}{k_n} I_{dc} \tag{5.2}$$

$$V_{ln_{pk}} = 0.294 \cdot k_n \cdot V_{dc} \tag{5.3}$$

The three-phase VA rating is calculated as:

$$\begin{aligned} VA_{pri} &= \frac{3}{\sqrt{2}} V_{ln_{pk}} I_s = \frac{3}{\sqrt{2}} 0.294 \cdot k_n \cdot V_{dc} \frac{1.6054}{k_n} I_{dc} \\ &= 1.001 V_{dc} I_{dc} \end{aligned} \tag{5.4}$$

Assuming a 5% safety margin in primary current for magnetising current and other losses and 10.15% increase due to $V_{no-load}$, the VA rating should be:

$$\begin{aligned} VA_{pri} &= 1.001 V_{dc} I_{dc} \times 1.05 \times 1.1015 \\ &= 1.15 V_{dc} I_{dc} = 222.18 \text{ VA} \approx 250 \text{ VA} \end{aligned}$$

The 12-pulse transformer (400 V : 50 V/50 V, $TWS - Christchurch$ make) used in this work was already available at the "Machines Laboratory" in the department. It was found suitable to be used for the proposed proof of concept based on the above calculations.

5.3 SELECTION OF POWER SEMICONDUCTORS

The choice of the thyristors depends on the average and RMS currents, on the peak voltages (forward and reverse), and on the peak current it may experience in case of short circuit of the load. The minimum peak voltage across the main bridge thyristor is $2 \times \sqrt{2} \times V_{LL_{sec}}(max) + 50\%$ for safety = 323 V. The average and RMS currents are:

$$I_{thy}(avg) = \frac{I_{dc}}{3} = \frac{1.4}{3} = 0.466 \text{ A}$$
$$I_{thy}(rms) = 0.576 \times I_{dc} = 0.806 \text{ A}$$

The following thyristor is used for this application.

Table 5.2: BT152800R Thyristor specifications for the Main Bridge.

No	V_{DRM} (V)	I_T (A)	V_F (V)	I_{GM} (A)	V_{RGM} (V)	$T_{jmax}(^\circ C)$
BT152R	800	13	1.75	5	5	125°

Using Eqn. 4.39, the maximum voltage that a reinjection switch is subjected to is found to be 166.9 V. The reinjection switches are fully controllable power semiconductor switches. They must have unidirectional current flow and bipolar voltage blocking capability. The different fully controllable power semiconductor switches are GTOs, IGBTs or IGCTs. Of these IGBTs are available in different configurations; Symmetrical IGBT, in which there is an anti-parallel free-wheeling diode in the same housing, and Asymmetrical IGBT, in which there is no anti-parallel free-wheeling diode. The Asymmetrical IGBT can be used if a fast recovery diode is placed in series to get bipolar voltage blocking capability. For reinjection applications, there is no need for the extra anti-parallel free-wheeling diode, hence an Asymmetrical IGBT is used. The following IGBT and diode combination is used for this application.

Table 5.3: IGBT and Diode specifications for Reinjection Bridge.

No	V_{DRM} (V)	I_C (A)	V_F (V)	E_{on} (mJ)	E_{off} (mJ)	$T_{jmax}(^\circ C)$
IXGP20N (Asym.)	1200	20	2	0.9	6.5	150°
STTH3012D	1200	20	1.3	–	–	175°
MUR860	600	8	1.5	–	–	175°

5.4 GENERATING OF FIRING PULSES FOR 12-PULSE CONVERTER

5.4.1 Ramp Generation

There are numerous approaches of designing the gate pulses at the required α. The purpose of writing this section to give an exhaustive treatment of the scheme used in this work to design the firing angle controller (FAC). The commonly used firing pulse generators are:

- The Cosine-Firing scheme
- Ramp Comparator scheme
- Equidistant Pulse Firing scheme

The ramp-comparator scheme is chosen for implementation due to its relative simplicity. Under a controlled laboratory environment, variation in voltages and frequency can be eliminated by using controllable AC voltage source. For a conventional thyristor based converter, it is well known how α is measured, giving it an effective range of $0° \leq \alpha \leq 180°$, [Kimbark 1971]. For a conventional thyristor based converter, if the gate current pulse is provided at a negative α, the outcome depends on the width of the gate current pulse. If pulse width is greater than the magnitude of α, it effectively means the gate pulse is being applied when incoming phase voltage is positive and the current transfer occurs at $\alpha = 0°$. If the width of the pulse is less than α, commutation between the phases will not occur. This effectively means $\alpha = 0°$ is the lower limit. Similarly, if $\alpha = 180°$, commutation voltage is zero and current continues to flow through the same thyristor. Therefore, for successful commutation, $\alpha < 180°$.

The desired ramp between $0° \leq \alpha \leq 180°$ is generated using the ramp-comparator approach as shown in Fig. 5.2. The zero crossing detector (ZCD) translates the input sensed voltage (V_{sensed}) into a square wave voltage (V_{sw}). When the rising zero crossing is detected, the capacitor charges, giving ramp rise of the voltage at the output (V_{ramp}) as shown in Fig. 5.3. And as soon as the square voltage is negative the capacitor discharges sharply and output is zero. On detecting the falling zero crossing, the capacitor voltage ramps up again. Adding these two voltages gives a triangular waveform as shown in Fig. 5.3. This triangular voltage is compared in the comparator with a variable reference DC voltage ($V_{control}$) to get the desired α. The value of α is varied by changing the value of $V_{control}$.

The advantages of this firing circuit is a linear and synchronised ramp voltage which can self-adjust the firing instant with frequency variation. The circuit depends only on the accurate zero crossing of V_{sensed}. Any change in frequency of the input signal will cause a corresponding change in the period of the ramp. Also, this method is not affected by line voltage fluctuations. However, this method is sensitive to false zero crossings. If there are variations in component

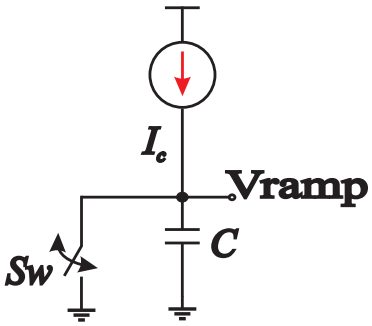


Figure 5.2: Capacitor based ramp generator.

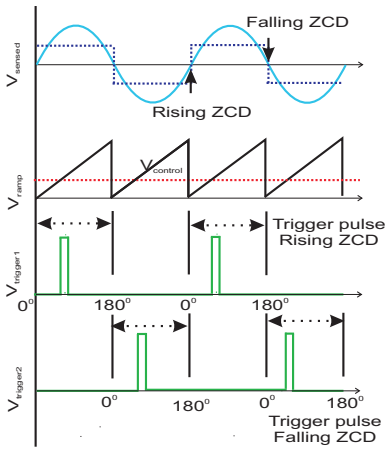


Figure 5.3: Ramp-Comparator scheme.

values of the ramp generator circuit and any noise voltage over V_{ramp} and $V_{control}$, these may cause improper firing. To avoid component value variation and reduce noise sensitivity, the gating signals are derived from the TCA785 control IC.

5.4.2 TCA785 based FAC

The TCA785 is a dedicated circuit for firing control of phase controlled devices. It is used to control the firing angle from 0° to 180°. Its configuration allows the selection of external components for the modification of firing pulse parameters. The block diagram of TCA 785 is given in Fig. 5.4.

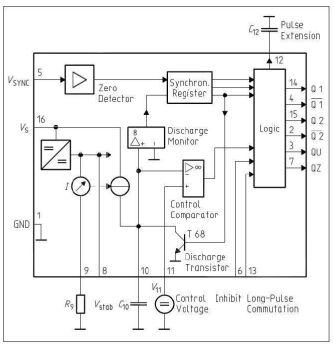


Figure 5.4: Block diagram of TCA785.

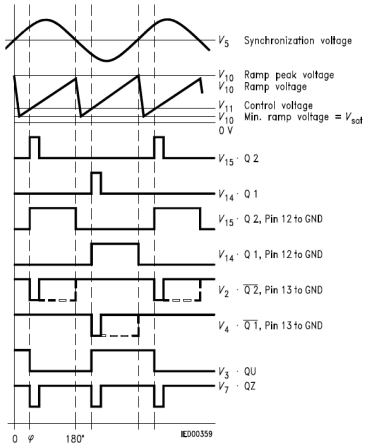


Figure 5.5: Pulse diagram of TCA785.

The level of the internal voltage (V_{ref}) is set at 3.1 V, which is used by the control system. Supply voltage V_{cc} is set at 15 V, with the maximum limit being 18 V. The synchronization is obtained through a zero detector, at pin 5, internally connected to a synchronization register.

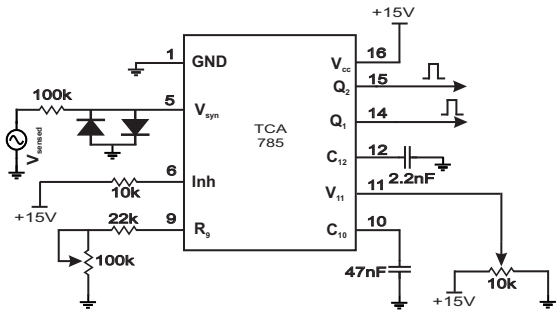


Figure 5.6: TCA 785 circuit diagram.

The ramp generator, whose control is in the logical unit, comes from a constant current source that charges the capacitor (C_{10}) connected at pin 10. This current (I_{10}) is controlled by a resistor or potentiometer (R_9) on pin 9. Its purpose is to adjust the amplitude of the ramp (V_{10}), which goes to zero when the voltage passes through the reference, due to the saturation of an internal transistor connected in parallel with the capacitor. The Control Comparator block compares the ramp voltage with the control voltage (V_{11}), and when ramp voltage exceeds the control voltage, the control comparator sends a signal to the logic unit. The logic unit generates a short pulse of duration 30 μs.

During the positive half cycle, this short pulse is obtained at pin 15 (Q2) and in a complementary manner, the pulse of the negative half-cycle is obtained at pin 14 (Q1). The width of these pulses are determined by connecting an external capacitor between pin 12 and the ground, and the amplitude is at V_{cc}. If pin 12 is connected to ground, then a firing pulse from α to 180° is obtained. At pins 2 ($\bar{Q}2$) and 4 ($\bar{Q}1$), the inverse or complementary outputs, from pins 14 and 15 respectively, are obtained. At pin 3 (QU), a square wave changing its level from α, $\pi+\alpha$...etc is obtained. This is used for controlling external logic. Pin 7 (QZ) performs the NOR operation of Q1 and Q2. Pin 6, when connected to ground, inhibits all outputs of the TCA 785. These waveforms are shown in Fig. 5.5.

TCA785 circuit diagram is shown in Fig. 5.6. The minimum and maximum values of charging current I_{10} is to be maintained between 10 μA and 1000 μA. The charging current is calculated as:

$$I_{10} = \frac{V_{ref} \times K}{R_9} \tag{5.5}$$

Here, $K = 1.1\pm$ 20%. From Eqn. 5.5, the value of R_9 can be calculated.

The ramp voltage must be maintained below (V_{cc}-2) V and is given by:

$$V_{10} = \frac{V_{ref} \times K \times t}{R_9 \times C_{10}} \tag{5.6}$$

With $V_{10} = 10$ V and $C_{10} = 47$ nF, $R_9 = 72.53$ kΩ. This gives $I_{10} = 47$ μA which is within the limit for I_{10}. From Eqn. 5.6, the value of C_{10} can be calculated where t = duration of the ramp. $t = 10$ ms for a 50 Hz waveform. Here, the maximum value of V_{11} must be at V_{10peak}. With V_{cc} = 15 V and $C_{12} = 1$ nF, the pulse width of TCA output is ≈ 580 μs/nF. $C_{12} = 2.2$ nF is used to obtain a pulse width = 1.2 ms ≈ 20°. The fabricated PCB for TCA785 is shown in Fig. 5.7. The ramp generation using TCA785 is tested with both perfect sinusoid and distorted voltages, obtained from the Programmable Chroma AC power source 61504 as shown in Fig. 5.8.

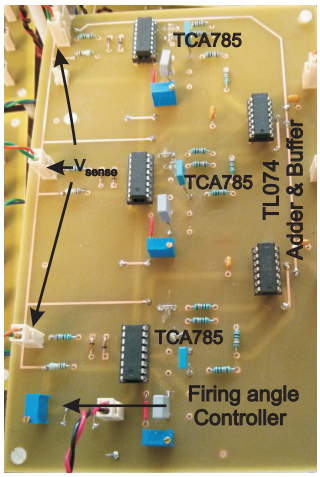


Figure 5.7: PCB for firing pulse generation using TCA785.

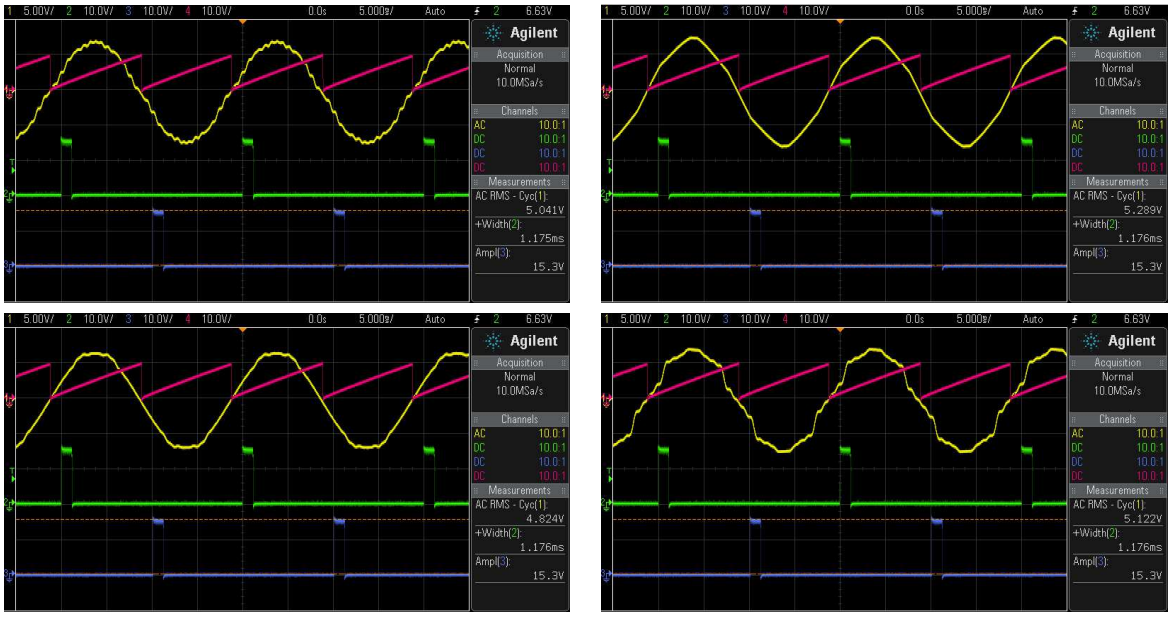


Figure 5.8: Ramp generation using TCA 785 under distorted input, Ch1: V_{sensed}, Ch2: V_{ramp}, Ch3: TCA output1, Ch4: TCA output2.

5.4.3 Voltage transducer circuit

Voltage sensors LEM LV 25-P (Fig. 5.10) are used to convert power level voltage into low level signals having 5 V_{rms}. The Hall effect transducers provide the isolation between the high power system and the control electronic circuit. For a 12-pulse converter, six voltage sensors are used. The voltages sensed are: V_{an}, V_{bn}, V_{cn}, V_{ab}, V_{bc} and V_{ca}. The synchronising voltage for Y-connected secondary voltage V_{ca_Y} is Y-connected primary voltage V_{ca_Y}. For D-connected secondary voltage V_{ca_D}, the synchronising voltage is Y-connected primary voltage $-V_{an_Y}$ as shown in Fig. 5.9.

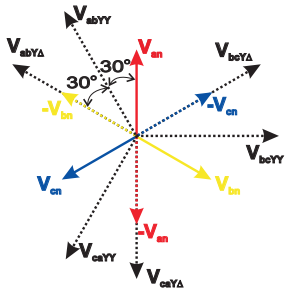


Figure 5.9: Line voltages for a Y-Y-D_{11} interface transformer.

Figure 5.10: Voltage sensor LEM LV25P.

The circuit diagram for LV-25P is shown in Fig. 5.11. For voltage measurements, a current proportional to the measured voltage is passed through the resistor R_{in}. For best accuracy of the transducer, R_{in} should be so selected that the voltage measured corresponds to a primary current ($I_{in_{rms}}$) of 10 mA. The current conversion ratio is 2.5, hence, the nominal secondary current is 25 mA.

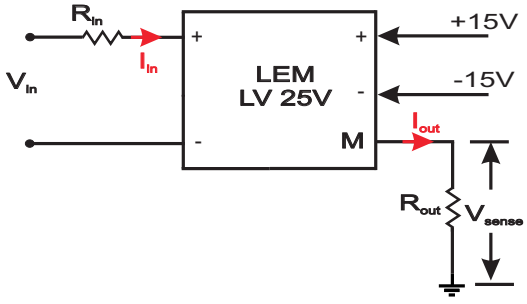


Figure 5.11: Hall effect voltage transducer.

The 12-pulse interface transformer rating is 400 V : 50 V. The primary side input resistance is calculated as:

$$R_{in} = \frac{400 \text{ V}}{10 \text{ mA}} \approx 40 \text{ k}\Omega. \tag{5.7}$$

A fixed value resistor of 40 kΩ/5 W is used. The output voltage (RMS) is set at 5 V. The output

resistance R_{out} is calculated as:

$$R_{out} = \frac{5 \text{ V}}{25 \text{ mA}} \approx 200 \ \Omega. \tag{5.8}$$

The maximum and minimum value of the measuring resistance R_{out} with a ± 15 V supply is between 100 Ω and 350 Ω. A variable 500 Ω/0.6 W resistor is used. The fabricated PCB for this purpose is shown in Fig. 5.12.

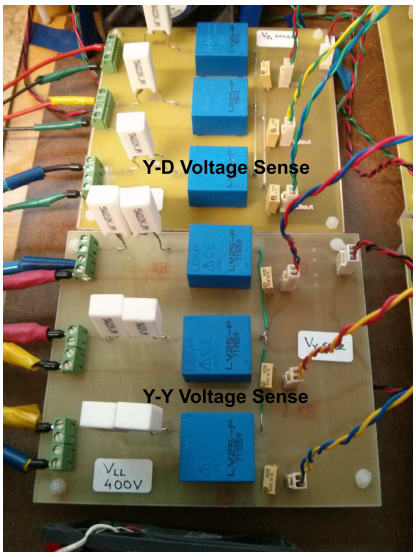


Figure 5.12: Voltage sensor PCBs for Y-Y and Y-D voltage sensing.

5.4.4 Thyristor driver circuit design

The gate circuit of a thyristor functions like a diode with high on state voltage drop and low reverse break down voltage. The important gate specifications of a thyristor are listed in the data-sheet. Some of these for the BT152800R thyristor include:

- *Gate trigger current* (I_{GT}): 32 mA, *Gate trigger voltage* (V_{GT}): 1.5 V
- *Non triggering gate voltage* (V_{GNT}): 0.2 V, *Peak reverse gate voltage* (V_{GRM}): 5 V
- *Peak gate trigger current* (I_{GM}): 5 A, *Peak gate trigger voltage* (V_{GM}): 5 V
- *Peak Gate Power dissipation*($P_{G_{(max)}}$) 20 W
- *Average Gate Power dissipation*($P_{G_{(av)}}$) 0.5 W
- *Gate controlled turn on time* (t_{on}): 2 μs

The thyristor V_{GM}, I_{GM} and $P_{G_{(av)}}$ limits cannot not be exceeded in order to avoid permanent damage to the gate cathode junction.

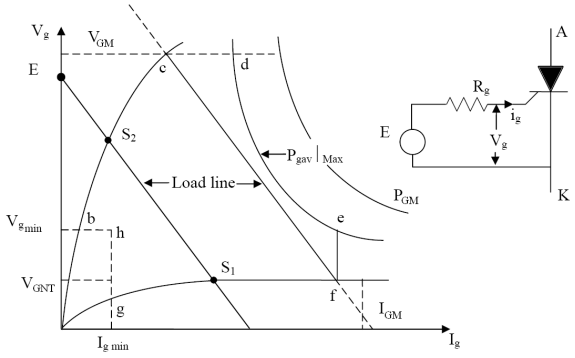


Figure 5.13: Gate characteristics of a thyristor.

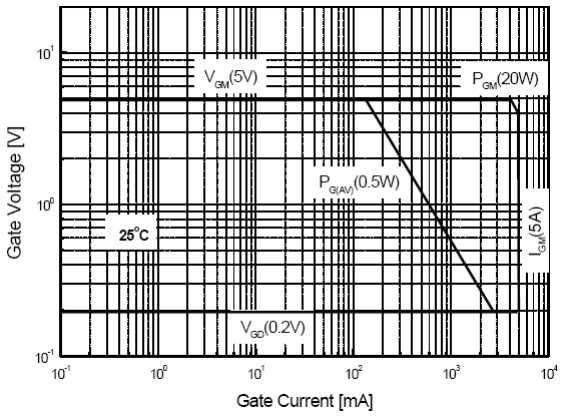


Figure 5.14: Gate characteristics of BT152.

Referring to Fig. 5.13, the operating point is decided by the load line given by:

$$\mathrm{V_g = E - R_g I_g} \tag{5.9}$$

For optimum utilization of the gate ratings the load line should be on the $P_{G_{(av)}}$ curve without violating V_{GM} or I_{GM} ratings. The actual gate characteristics for BT152R is shown in Fig. 5.14. With $V_{GM} = 5$ V, the gate load line i.e. $\mathrm{V_g = E - R_g I_g = 5 - R_g I_g}$ should be tangent to the $P_{G_{(av)}}$ or $P_{G_{max}}$ curve.

Thyristors are usually triggered using pulsed voltage and current. $P_{G_{max}}$ curve for pulsed operation allows higher gate current to flow which in turn reduces the turn on time of the thyristor. A duty cycle, $\delta = 50\%$ in the pulsed voltage and current waveform, $P_{G_{(av)}}$ curve is used. Let $\mathrm{V_{g_{op}}}$ and $\mathrm{I_{g_{op}}}$ be the operating point on the $P_{G_{(av)}}$ curve such that:

$$\mathrm{V_{g_{op}} = 5 - R_g I_{g_{op}}} \tag{5.10}$$

$$\mathrm{V_{g_{op}} I_{g_{op}} = 0.5} \tag{5.11}$$

Since Eqn. 5.10 is a tangent to Eqn. 5.11 at $V_{g_{op}}$ and $I_{g_{op}}$, the slope is -$\mathrm{R_g}$.

$$\left[\frac{dV_g}{di_g}\right]_{V_{g_{op}}, I_{g_{op}}} = -\mathrm{R} = -\frac{\mathrm{V_{g_{op}}}}{\mathrm{I_{g_{op}}}} \tag{5.12}$$

Solving Eqns. 5.10 and 5.11 gives $\mathrm{I_{g_{op}}} = 200$ mA, $\mathrm{V_{g_{op}}} = 2.5$ V, and $\mathrm{R_g} = 12.5\ \Omega$. Among the many ways to drive a thyristor, the pulse transformer is one of the easiest. For a given pulse transformer, the voltage-time product (Et) of the output pulse is constant. The pulse transformer used is the (1:1:1) 77205C (Fig. 5.16) from Murata Power Solutions. This pulse

transformer has Et constant = 240 Vμs. In practice the area of the pulse is lower than 60-70% of the maximum Et product. The maximum pulse duration available in the gate will be:

$$t_{pulse} = \frac{0.6 \cdot 240 \text{ V}\mu\text{s}}{2.5} = 57 \ \mu\text{s} \tag{5.13}$$

The pulse duration (t_p) can now be chosen between $t_{on} \leq t_p \leq t_{pulse}$. Frequency range from 5 kHz to 70 kHz is tested with $\delta = 50\%$ and $t_p = 7.14$ μs (pulse frequency is 70 kHz) is implemented. This gives $P_{G_{max}} = \frac{P_{G(av)}}{f \cdot t_p} \approx 1 \text{ W} \leq 20 \text{ W}$.

5.4.5 Generating a High Frequency Pulse Train

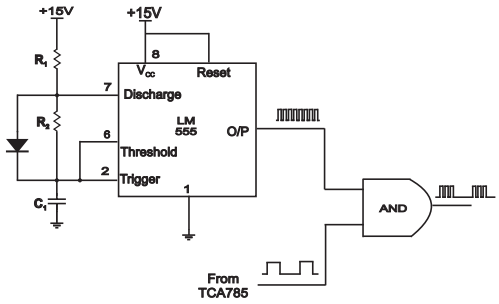


Figure 5.15: High frequency pulse train using LM555.

Figure 5.16: Pulse transformer 77205C.

LM555 timer is used to generate the high frequency pulse train as shown in Fig. 5.15. The component values for LM555 are: $R_1 = R_2 = 10$ kΩ and $C_1 = 1$ nF, resulting in a frequency ≈ 70 kHz (T = 1.4RC). This high frequency pulse train, with a duty cycle of 50% is applied to an AND gate (4081) continuously along with the triggering pulse from the TCA785. The pulse train is allowed to reach the gate of the thyristor driver circuit only when the triggering pulse is high, as shown in Fig. 5.17.

Figure 5.17: Ch1:V_{sensed}, Ch2:TCA output1, Ch3:TCA output2, Ch4:ANDing TCA output2 and LM555.

5.4.6 Forward converter based thyristor driver circuit

The thyristor driver circuit is based on the forward converter topology with isolation between the control and power circuit being provided by the 77205C pulse transformer.

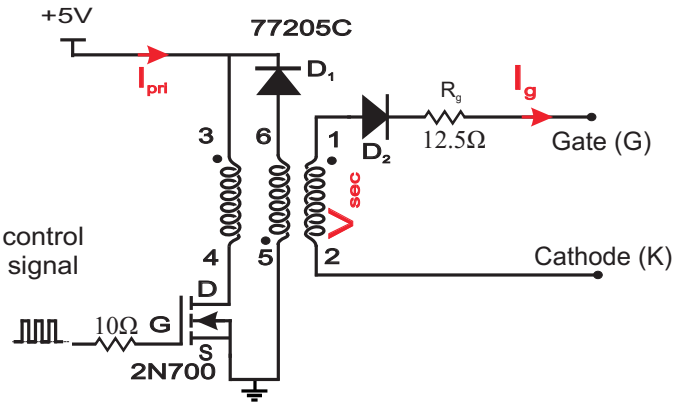


Figure 5.18: Forward converter based thyristor driver circuit.

When the MOSFET is on, diode D_2 conducts and $V_{sec} = 5$ V is available across the secondary winding of the pulse transformer. V_{sec} drives gate current I_g in the gate-cathode junction of the thyristor to turn it on. For $I_g \approx 200$ mA, the gate drive resistor $R_g = 12.5\ \Omega$. When the MOSFET is off, diode D_1 returns the energy stored in the pulse transformer back to the supply.

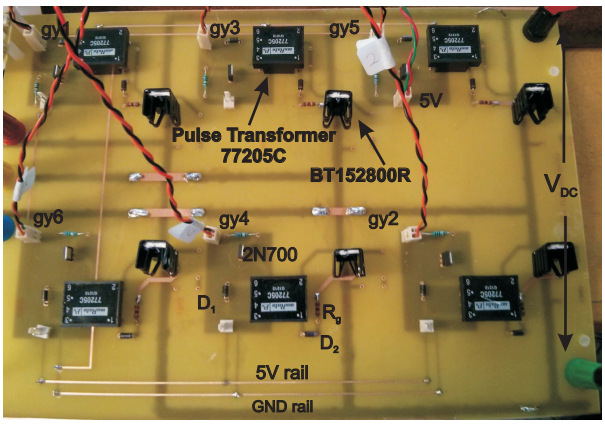


Figure 5.19: 6-pulse phase controlled Thyristor converter PCB.

5.4.7 Heat Sink Calculation for Thyristors

For thyristors and diodes, the dissipation (or losses) are classified as off-state, on-state, turn-on and turn-off losses. The thyristor also shows control losses. However, for mains operation, the dimensioning can be exclusively done based on the on-state losses, as the sum of the others is comparatively negligible. In the thyristor data-sheet, the total power dissipation (P_{tot}), which is average value of the sum of the individual losses, is specified. The average value of the on-state

loss P_{av} is calculated with the values of the equivalent straight line according to the following formula:

$$P_{av} = V_{T(TO)} \times I_{Tav} + r_T \times I_{Tav}^2 \times F^2 \tag{5.14}$$

where $V_{T(TO)}$: threshold voltage, r_T: slope resistance, I_{Tav}: average on-state current, F: form factor.

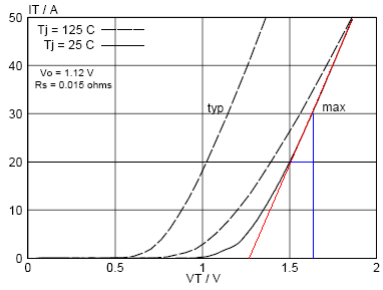


Figure 5.20: V-I characteristics of BT152800R.

From Fig. 5.20, $V_{T(TO)} = 1.12$ V and $r_T = 0.015\ \Omega$. For a general 6-pulse converter, the current through any thyristor can be considered as a square wave of on-duration (t_{on}) 120° (6.66 ms) and time period (T) of 20 ms. Assuming a peak current (I_{pk}) of 5 A, the average current I_{Tav} is 0.333×5 = 1.665 A. The form factor (F) for a 120° square wave = $\sqrt{3}$. Substituting the values in Eqn. 5.14, the on-state loss P_{av}: 2.23 W. Heat sink calculation is based on:

- The maximum operating junction temperature, $T_j = 125°$.
- Ambient temperature, $T_a = 25°$.
- Thermal resistance from junction to case, $R_{jc} = 1.1$ °C/W. (using BT152800R thyristor)
- Thermal resistance from case to heat sink with silicone compound , $R_{cs} = 0.5$ °C/W.
- Thermal resistance from heat sink to ambient, $R_{sa} = 21$ °C/W. (using the FK237SA220 heat sink)

The maximum power that the thyristor can be allowed to dissipate (so that the temperature rise is below the maximum permissible limit) is:

$$P_d = \frac{T_j - T_a}{R_{jc} + R_{cs} + R_{sa}} = \frac{125 - 25}{(1.1 + 0.5 + 21)} = 4.42 \text{ W} \tag{5.15}$$

This means that the thyristor can dissipate ≈ 4.5 W before it overheats, which is above P_{av}: 2.23 W. The choice of FK237SA220 heat sink is justified.

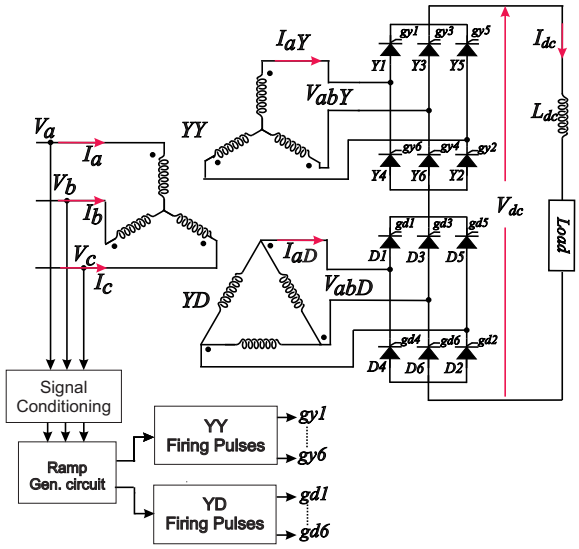


Figure 5.21: Thyristor based 12-pulse converter.

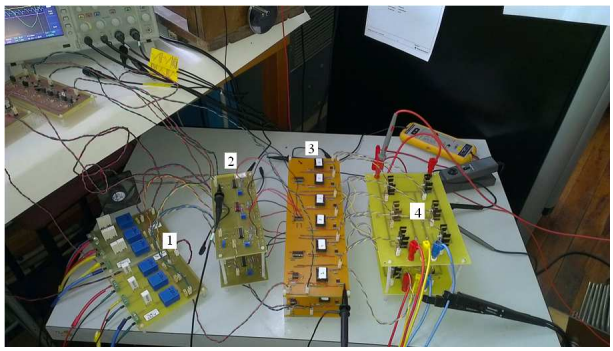


Figure 5.22: Pre-PCB test-board: 1. Voltage sensor, 2. TCA785 controller, 3. 77205C based gate driver 4. BT152800R based converter.

5.5 THYRISTOR BASED 12-PULSE CONVERTER EXPERIMENTAL RESULTS

This section presents the test results for a 12-pulse main bridge converter ((Fig. 5.21) prototype (initial test-board before PCB was fabricated is shown in Fig. 5.22) designed. With $R_{dc} = 50\ \Omega$ and $\alpha \approx 15^\circ$, the overlap angle μ, in terms of impedance parameters is calculated as [Shepherd and Zhang 2004]:

$$\mu = \cos^{-1}\left(\frac{1-(3/\pi)\omega L_s/R_{dc}}{1+(3/\pi)\omega L_s/R_{dc}}\right) \text{ for } \mu < 60^\circ \tag{5.16}$$

The average output voltage V_{dc} is [Shepherd and Zhang 2004]:

$$V_{dc} = 2 \times \frac{1.65\dfrac{V_{pk}}{k_n}\cos(\alpha)}{1+\dfrac{3\omega L_s}{\pi R_{dc}}} \tag{5.17}$$

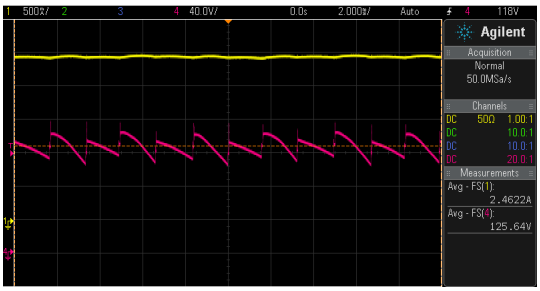
The average load current I_{dc} is calculated as:

$$I_{dc} = \frac{V_{dc}}{R_{dc}} \tag{5.18}$$

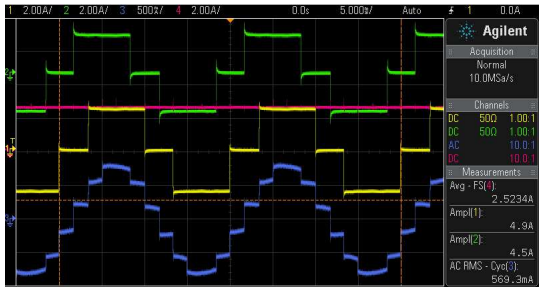
Using Eqns. 5.18 and 5.17, $V_{dc} \approx 126.21$ V and $I_{dc} \approx 2.525$ A is obtained, whereas actual results obtained are shown in Fig. 5.23.

RMS value of the fundamental component (I_{a1rms}) of AC-side line current I_a is:

$$I_{a1rms} = \frac{1.5594}{8} \times 2.5 \approx 0.4873 \text{ A} \tag{5.19}$$



12-pulse converter V_{dc} and I_{dc} waveforms.



I_{aY}, I_{IaD}, I_{dc} and I_a waveforms.

Figure 5.23: 12-pulse Thyristor controlled converter results, $\alpha = 15°$.

Similarly, RMS value of the AC-side line current $I_{a_{rms}}$ is

$$I_{arms} = \frac{1.5767}{8} \times 2.5 \approx 0.4927 \text{ A} \tag{5.20}$$

Using Eqns. 5.19 and 5.20, the calculated THD is 14.9% whereas measured THD is 16.32%.

5.6 MODIFICATION OF THE FIRING ANGLE CONTROLLER FOR MLCR APPLICATIONS

In the previous section it is mentioned that the range of α is between $0° \leq \alpha \leq 180°$. For thyristor based MLCR CSC, it needs to be modified to achieve α in the range of $-180° \leq \alpha \leq 180°$. This is done by modifying the ramp-comparator FAC. The trigger pulse **gy1** (Fig. 5.17) is synchronised to the falling zero crossing of V_{ca}. To extend the firing angle in the negative range, the trigger pulse **gy1** must be synchronised to the rising zero crossing of V_{ca} as shown in Fig. 5.24.

This modification is described in the following subsections:

5.6.1 Zero crossing detector

The LM318 operational-amplifier (op-amp) is used as the zero crossing detector (ZCD), as shown in Fig. 5.25. The synchronised voltage signal and reference ground signal are given to the non-inverting terminal and inverting terminal of the op-amp respectively. +15 V DC is given to pin 7 and -15 V DC is given to pin 4. The op-amp compares the voltage signal with the ground signal. When the instantaneous value of the voltage signal is higher than the reference signal, the output of the op-amp goes to $+V_{cc}$ and vice-versa, producing a square wave. The diode (1N914) cuts the negative part of the square wave, and an unipolar square wave is obtained, which is then fed to a frequency divider circuit. To obtain both the positive and the negative zero crossings, the

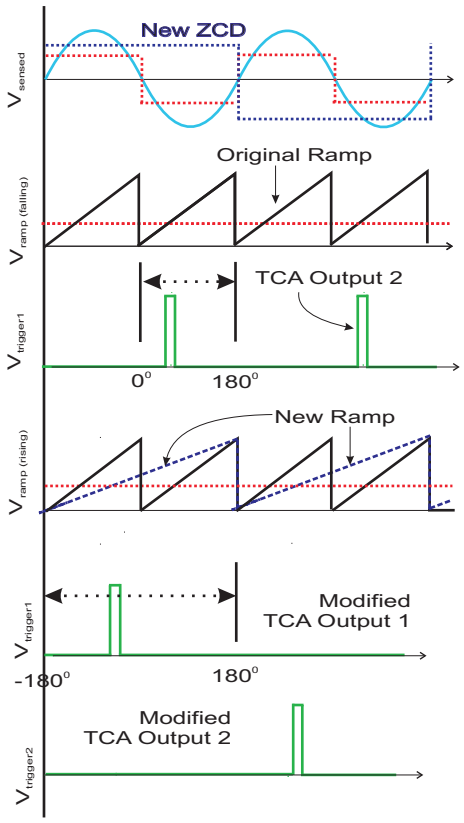


Figure 5.24: FAC modification and extension to −180°.

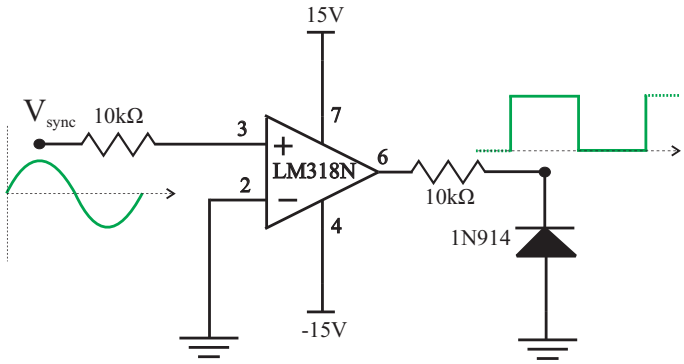


Figure 5.25: Simple zero crossing detector using LM318.

ZCD output is fed to the frequency divider via a non-inverting buffer HEF4050 and an inverting buffer HEF4049.

5.6.2 Frequency divider circuit

The frequency divider circuit is constructed from the D-flip flop 74LS74 (Fig. 5.26). The output from pin 6 ($\bar{Q}$) is connected to the input pin 2 (D), and the output pulses at pin 5 (Q) have a frequency that is exactly half that of the input clock frequency.

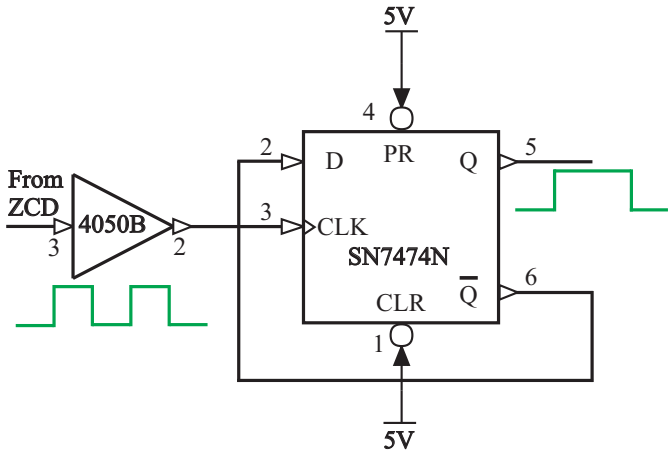


Figure 5.26: Frequency divider circuit using SN7474.

5.6.3 Unipolar to Bipolar signal conversion

As the TCA785 only accepts a bipolar signal, the unipolar signal with half the input frequency needs to be converted to a bipolar signal. The main requirements from this circuit are:

- When input voltage = 0 V, output voltage = -5 V.
- When input voltage = 5 V, output voltage = 5 V.

From this requirement it is observed that the gain of the amplifier has be 2 with an offset of -5 V. A differential amplifier as shown in Fig. 5.27 is implemented. The transfer function for this amplifier is given as:

$$V_{out} = V_1(1 + \frac{R_2}{R_1}) - V_2(\frac{R_2}{R_1}) = 2V_1 - 5 \tag{5.21}$$

with $R_1 = 10$ kΩ, $R_2 = 10$ kΩ and $V_2 = 5$ V.

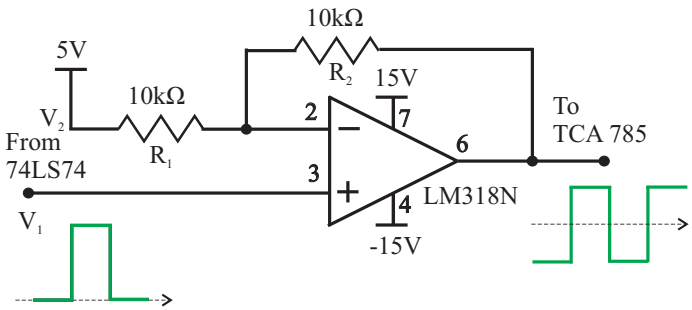


Figure 5.27: Bipolar signal conversion using LM318.

Two PCBs are fabricated for zero-crossing detection, frequency division and unipolar to bipolar signal conversion for the Y-Y and Y-D sensed voltages. One of the PCBs is shown in Fig. 5.28.

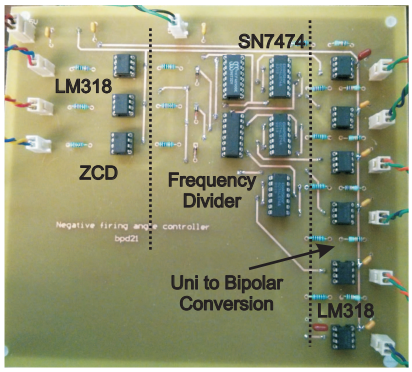


Figure 5.28: PCB for zero-crossing detection, frequency division and unipolar to bipolar signal conversion.

5.6.4 TCA785 modification

As the ramp time $t = 20$ ms in this case, using $V_{10} = 10$ V and $C_{10} = 220$ nF in (5.6) gives $R_9 = 31$k Ω. This gives $I_{10} = 110$ μA which is within the limit for I_{10}. The TCA 785 circuit is shown in Fig. 5.29 and the modified FAC ramp is shown in Fig. 5.30.

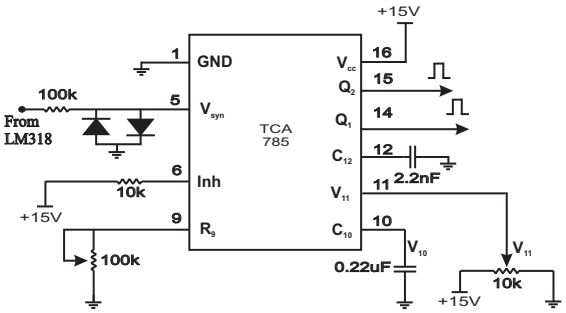


Figure 5.29: TCA 785 circuit diagram.

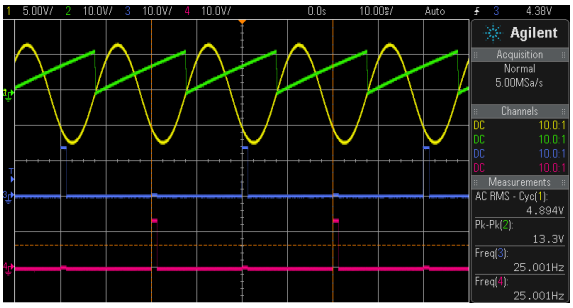


Figure 5.30: Ch1: V_{sensed}, Ch2: V_{ramp} at rising ZCD, Ch3: TCA output1, Ch4: TCA output2.

5.6.5 Voltage adder

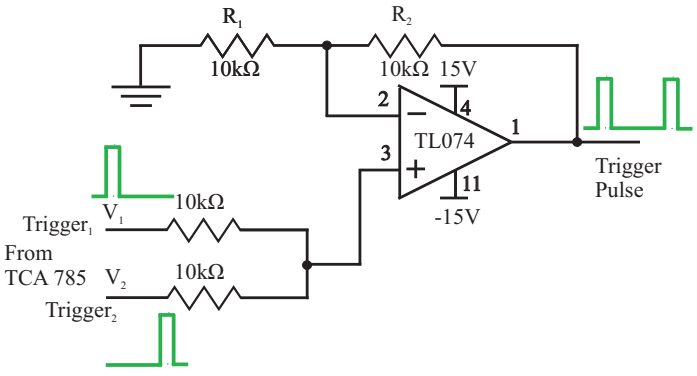


Figure 5.31: Voltage adder circuit using TL074.

The two trigger pulses are added together using a voltage adder circuit as shown in Fig. 5.31. Addition is necessary to revert back to the source frequency. The extension of α to 180° for both falling and rising ZCDs are shown in Figs. 5.32 and 5.33. With a voltage divider composed of a 10 kΩ/10 kΩ combination, the non-inverting adder has a voltage gain of 2. With two input voltages having equal input resistance, the voltage at the V_+ is $V_1 + V_2$ with a gain of 2 .

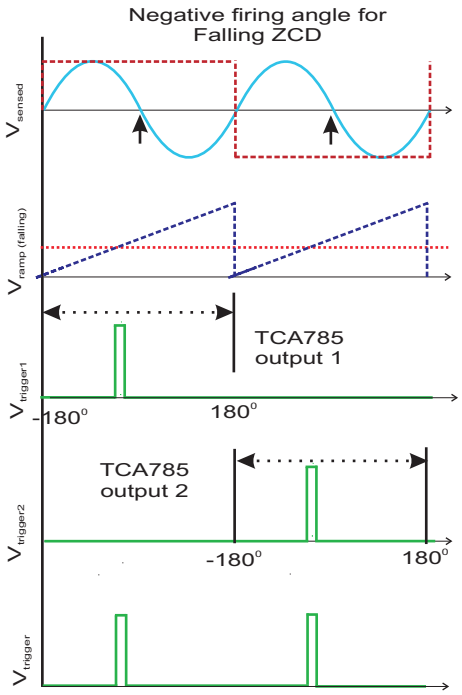


Figure 5.32: Extension of α for falling ZCD.

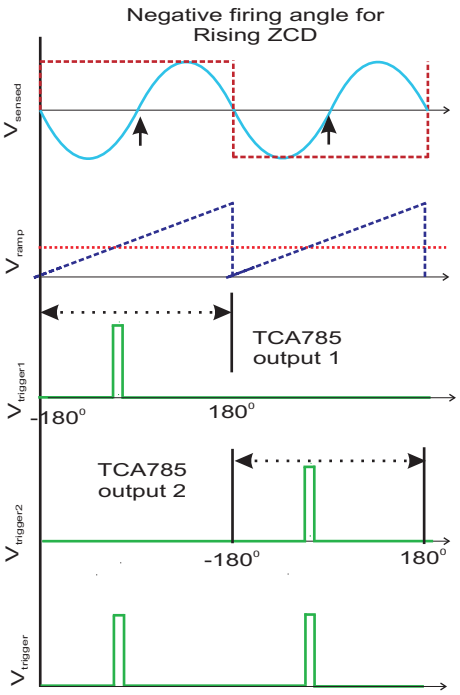


Figure 5.33: Extension of α for rising ZCD.

Trigger pulse between $-180° \leq \alpha \leq 180°$ is shown in Figs. 5.34 and 5.35.

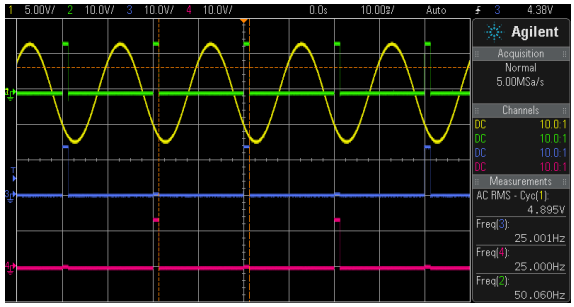


Figure 5.34: Ch2: Trigger pulse in $0° \leq \alpha \leq 180°$.

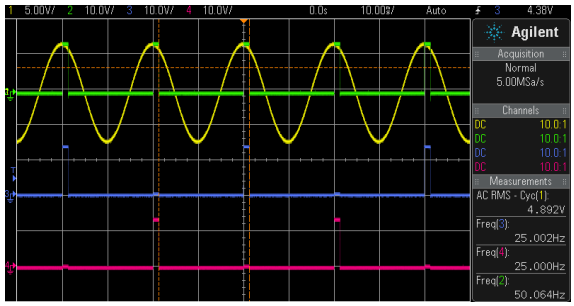


Figure 5.35: Ch2: Trigger pulse in $-180° \leq \alpha \leq 0°$.

5.7 GENERATING OF REINJECTION PULSES FOR 3-LEVEL MLCR

This section illustrates the generation of reinjection pulses for 3-level reinjection bridge based on the firing pulses for the main bridge. Section 5.7.1 presents the selection of IGBT driver circuit.

The firing sequence for 3-level MLCR CSC is shown in Fig. 4.15. In order to produce the firing sequence needed to generate the 3-level I_{inj}, the firing sequence of the reinjection IGBTs are synchronised with the main bridge switching. The derivation of reinjection pulses for each switch pair are shown in Figs. 5.36 and 5.37. In Fig. 5.36 it is shown that each reinjection turn-on pulse is delayed from the main bridge switching pulse by 52.5°, and the width of the turn-on pulse is 15°. Based on the six main bridge switching pulses, six reinjection turn-on pulses are derived, which are then added together to form the reinjection pulse for reinjection IGBT pair $Sp1/Sn1$. Following a similar procedure, the reinjection pulse for reinjection IGBT pair $Sp2/Sn2$ is also derived as shown in Fig. 5.37.

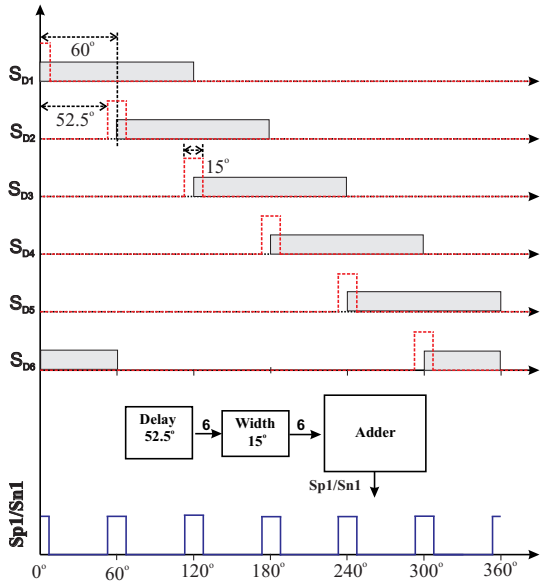


Figure 5.36: Generation of reinjection pulse for reinjection IGBT $Sp1/Sn1$.

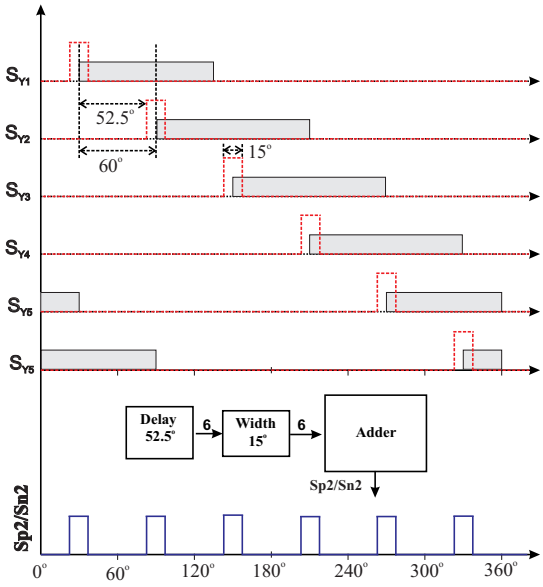


Figure 5.37: Generation of reinjection pulse for reinjection IGBT $Sp2/Sn2$.

5.7.1 IGBT driver circuit

The switching behaviour of an IGBT is determined mainly by its capacitances (charges) and the internal and outer resistances. The internal resistance is omitted in the IXYS data-sheet because its value is much lower in magnitude, and has very little influence on the switching time, hence only the gate resistance R_g is considered. Together with IGBT input capacitances, R_g forms an RC network that determines the voltage change at the IGBT gate and thus the switching time. IGBT IXGP20N is used for this purpose and has the following characteristics (Table 5.4):

Table 5.4: Specifications for IXGP20N.

Parameter	Designation	Values
$C_{ies} = C_{ge} + C_{gc}$	Input Capacitance	1750 pF
$C_{res} = C_{gc}$	Rev. transfer Capacitance	90 pF
$C_{oes} = C_{gc} + C_{ce}$	Output Capacitance	31 pF
Q_G	Gate charge	63 nC
$V_{GE}max$	Gate-Emitter voltage	±20 V

Usually the gate charge Q_G needed to drive the IGBT can be determined using the gate charge characteristic diagram, which is mostly specified in the data-sheet. If the gate-charge curve is not specified, then an approximate method for determining the gate charge using the C_{ies} and gate capacitance factor k_c can be employed. However, this method is not entirely accurate. The individual power of the driver circuit needed to drive the IGBT can be found as a function of the intended switching frequency and the energy that has to be used to charge and discharge the IGBT. The driver output power (P_O) is given by:

$$P_O = P_{O(bias)} + P_{O(switch)} = I_{cc} \times \Delta V_{GE} + \Delta V_{GE} \times Q_G \times f_{sw} \tag{5.22}$$

where

- $P_{O(bias)}$ = Steady-state power in driver due to device biasing.
- $P_{O(switch)}$ = Driver power for charging and discharging of IGBT gate capacitance.
- I_{cc} = Supply current to power internal circuitry = 5 mA
- $\Delta V_{GE} = V_{G(on)} - VG_{(off)}$ = 15 V as $VG_{(off)}$ = 0 V as negative voltage supply is not used.
- f_{sw} = switching frequency = 300 Hz (Reinjection frequency)

Using the above information, P_O is calculated as:

$$\begin{aligned} P_O &= (5 \text{ mA} \times 15 \text{ V}) + (15 \text{ V} \times 63 \text{ nC} \times 300 \text{ Hz}) \\ &= 75 \text{ mW} < 370 \text{ mW} \quad \text{for ACPL312T} \end{aligned}$$

The driver input power (P_I) is given by:

$$P_I = I_{F(on)} \times V_{Fmax} \tag{5.23}$$

where

- $I_{F(on)}$ = Forward-current of IGBT driver (ACPL312T) = 16 mA.
- V_{Fmax} = forward voltage drop of IGBT driver (ACPL312T) = 1.95 V.

Using the above information, P_I is calculated as:

$$P_I = (16 \text{ mA} \times 1.95 \text{ V}) = 31.2 \text{ mW}$$

Hence, total power dissipation P_{tot} = 106.2 mW < 400 mW for ACPL312T. The absolute maximum power dissipation rating has not been exceeded and this justifies the use of ACPL312T for this application in terms of gate-drive power requirements. Another key requirement for IGBT driver circuits is that enough current can be supplied to charge and discharge the input capacitances of the IGBT and thus switch the IGBT on and off. This gate current is the minimum average output current of the driver, which is calculated as:

$$I_G = Q_G \times f_{sw} = 63 \text{ nC} \times 300 \text{ Hz} = 19 \ \mu\text{A}$$

The peak gate current with $\mathrm{R_g}$ = 10 Ω is calculated as:

$$I_{Gpeak} = \frac{\Delta V_{GE}}{\mathrm{R_g}} = \frac{15 \text{ V}}{10 \ \Omega} = 1.5 \text{ A} \ < \ 2.5 \text{ A of ACPL312T}$$

The response of the opto-coupler depends on the value of gate resistance $\mathrm{R_g}$ and can also be calculated by assuming I_{Gpeak} = 2.5 A with V_{OL} obtained from data-sheet.

$$\mathrm{R_g} \geq \frac{V_{cc} - V_{OL}}{I_{OL_{peak}}} = \frac{15 \text{ V} - 3.5 \text{ V}}{2.5 \text{ A}} = 4.6 \ \Omega. \tag{5.24}$$

The value of R_g has a significant impact on the dynamic performance of IGBTs. A smaller gate resistor charges and discharges the power transistor input capacitance faster, reducing switching times and switching losses. The trade off is that this could lead to higher voltage oscillations. Since the maximum peak gate current of the driver must be equal to or higher than maximum calculated peak gate current, choosing $R_g = 10\ \Omega$ is a good trade-off.

Once the logical signals are available, these are fed to the IGBT driver circuit. The isolated gate driver ACPL312T is used for this purpose as mentioned earlier. The driver circuit is shown in Fig. 5.38. Since there are six switches in the reinjection bridge, six isolated DC-DC converters are required. The isolated DC-DC converter 0515S from Tracopower is used. $V_{cc} = 15$ V is chosen because the output voltage V_o goes high when the LED is on with $V_{cc} - V_{ee}$ between 13.5 - 30 V. The high logic level of input voltage from SR-FF = 5 V is converted to 15 V. Input resistance R_{in} is calculated (I_{in} must be between 7 mA - 16 mA) as:

$$R_{in} = \frac{15\ \text{V} - 1.5\ \text{V}}{10\ \text{mA}} \approx 1.5\ \text{k}\Omega. \tag{5.25}$$

A decoupling capacitor of 0.1 μF is placed across V_{cc} and V_{ee}, very close to the opto-coupler itself to filter out any noise coming from the isolated DC-DC converter.

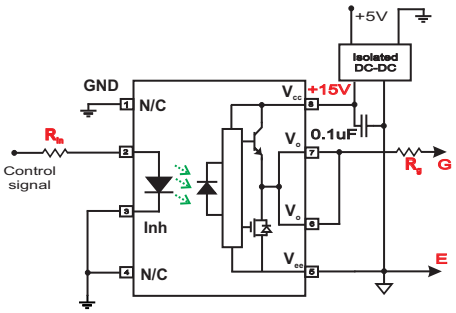


Figure 5.38: ACPL312T IGBT driver circuit.

5.7.2 Heat Sink Calculation for IGBT

A simplified method of calculating the power dissipation of IGBT switch is used, where the losses are classified as on-state, turn-on and turn-off loss. The average value of the IGBT power loss (P_l) is calculated according to the following formula:

$$\begin{aligned} P_l &= \text{On-state loss} + \text{Turn-on loss} + \text{Turn-off loss} \\ &= \frac{t_{on}}{T} \times V_{ce(sat)} \times I_c + f_{sw} \times (E_{on} + E_{off}) \end{aligned} \tag{5.26}$$

where $V_{ce(sat)}$: saturation voltage, I_c: On-state current, f_{sw}: switching frequency and the switch-

ing energy: $(E_{on} + E_{off})$.

Power loss calculation is based on: $V_{ce(sat)}$: 2.5 V, I_c: 2 A, f_{sw}: 300 Hz, E_{on}: 0.9 mJ, E_{off}: 9.5 mJ, the maximum operating junction temperature, $T_j = 150°$.

On-state loss, $P_{on} = 0.33\times$ 2.5 V$\times$ 2 A = 1.65 W and switching loss, $P_{sw} = 300$ Hz$\times$ 8.55 mJ = 2.56 W. Hence, $P_l = 4.21$ W. Thermal resistance from junction to case, $R_{jc} = 0.83$ °C/W for IXGP20N IGBT. Using FK237SA220, maximum power loss before the IGBT overheats is 5.6 W. The use of the same heat sink for thyristors and IGBT is justified. A 12 V DC fan is used for forced air cooling.

5.7.3 Reinjection pulse generation using 74LS123

The 74LS123 dual retriggerable monostable multi-vibrator is a one-shot device capable of very long output pulses. External components R_{ext} and C_{ext} are used as timing components to determine the output pulse duration. C_{ext} may vary from 0 pF to any necessary value. The basic output pulse duration is essentially determined by the following formula (where K varies as shown in Fig. 5.39):

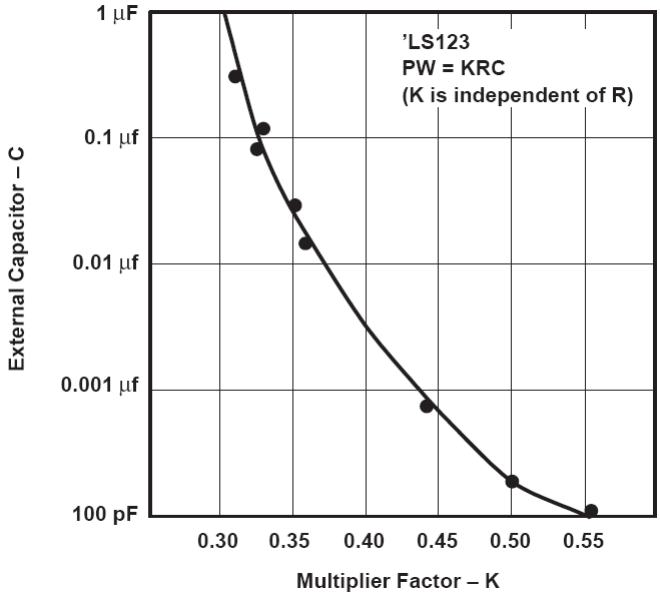


Figure 5.39: Multiplier Factor (K) vs C_{ext} for 74LS123.

$$t_w = K \times R_{ext} \times C_{ext} \tag{5.27}$$

For $C_{ext} \geq 1$ μF, the output pulse duration t_w ($K = 0.33$) is:

$$t_w = 0.33 \times R_{ext} \times C_{ext} \tag{5.28}$$

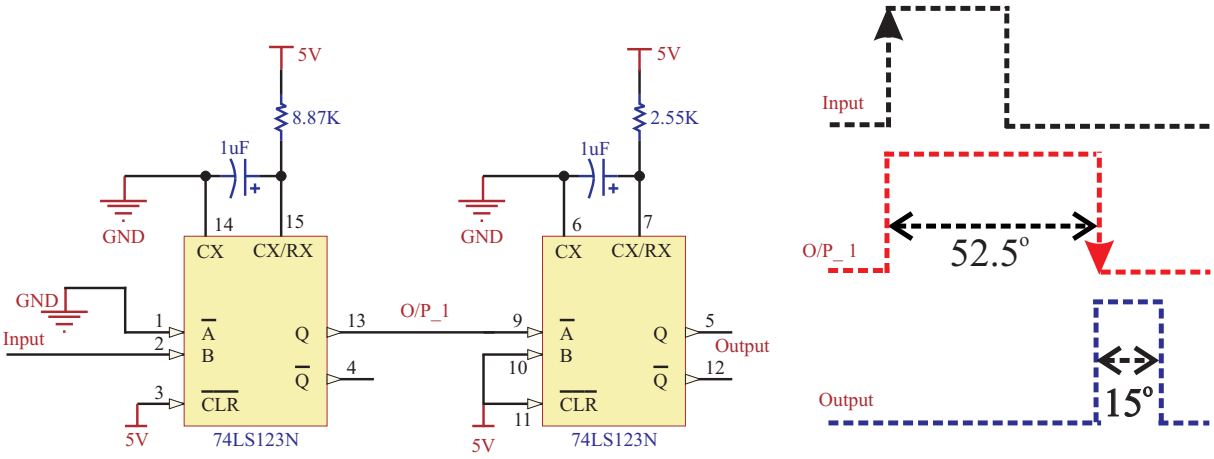


Figure 5.40: Using 74LS123 to generate reinjection pulses $Sp1/Sn1$ and $Sp2/Sn2$.

For a delay of 52.5° equal to 2.917 ms, $C1_{ext}$ = 1 μF and $R1_{ext}$ = 8.81 kΩ is needed as the external timing components for 74LS123. The rising edge of the main bridge switching signal is detected by the 74LS123 and it produces an output pulse for 2.91 ms wide. The other half of the 74LS123 is configured as a falling edge detector to detect the falling edge of the output of the first half and produce a pulse which is 15° (833 μs) wide. Here, $C2_{ext}$ = 1 μF and $R2_{ext}$ = 2.53 kΩ is needed. This is shown in Fig. 5.40. The closest values for timing components needed and available (1% tolerance value is used) are listed in Tables 5.5 and 5.6 which specifies the variation in timing delay and pulse width:

Table 5.5: Variation in timing delay due to $C1_{ext}$ and $R1_{ext}$ tolerances.

	Desired	Actual Mean	Actual Min.	Actual Max.	Tolerance
K	0.33	0.33	0.33	0.33	Assumed constant
$R1_{ext}$	8.81 kΩ	8.87 kΩ	8.78 kΩ	8.95 kΩ	1%
$C1_{ext}$	1 μF	1 μF	0.99 μF	1.01 μF	1%
t_w	2.917 ms	2.93 ms	2.86 ms	2.98 ms	–
Delay	52.5°	52.75°	51.5°	53.6°	–

Table 5.6: Variation in pulse width of $Sp1/Sn1$ and $Sp2/Sn2$ due to $C2_{ext}$ and $R2_{ext}$ tolerances.

	Desired	Actual Mean	Actual Min.	Actual Max.	Tolerance
K	0.33	0.33	0.33	0.33	Assumed constant
$R2_{ext}$	2.53 kΩ	2.55 kΩ	2.52 kΩ	2.57 kΩ	1%
$C2_{ext}$	1 μF	1 μF	0.99 μF	1.01 μF	1%
t_w	833μs	841.5 μs	823.3 μs	856.6 μs	–
Delay	15°	15.15°	14.8°	15.4°	–

5.7.4 Reinjection pulse adder for reinjection switch Sp1/Sn1 and Sp2/Sn2

The six delayed reinjection pulses are added together using a voltage adder circuit as shown in Fig. 5.41. With a voltage divider composed of a 10 kΩ/ 50 kΩ combination, the non-inverting

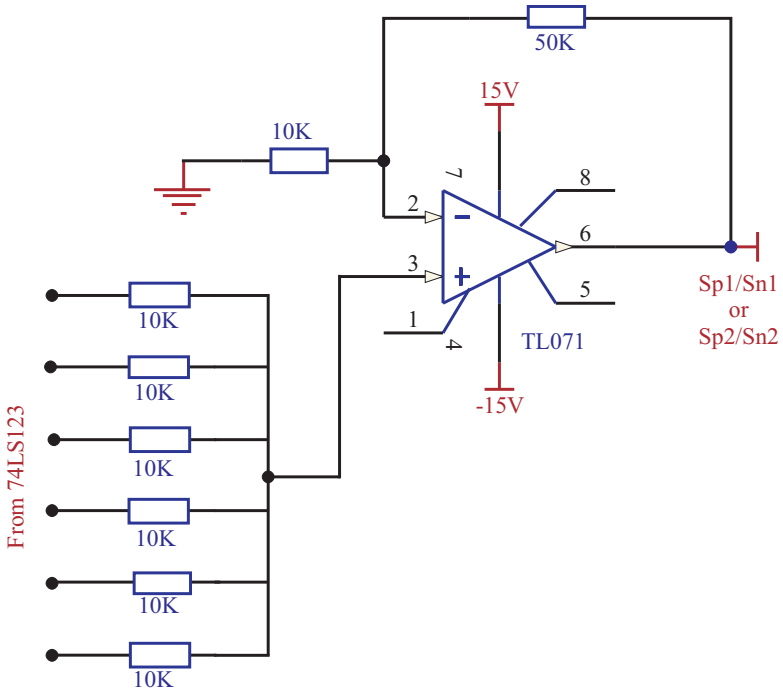


Figure 5.41: Non-inverting adder with voltage gain of 6.

adder has a voltage gain of 6. With two input voltages having equal input resistance, the voltage at the output is the sum of all the inputs from the 74LS123. HEF4050 hex non-inverting buffer is used between 74LS123 and TL071 to convert 5 V logic to 15 V logic for proper addition to obtain the reinjection pulses $Sp1/Sn1$ and $Sp2/Sn2$.

5.7.5 Reinjection pulse for reinjection switch Sp0/Sn0

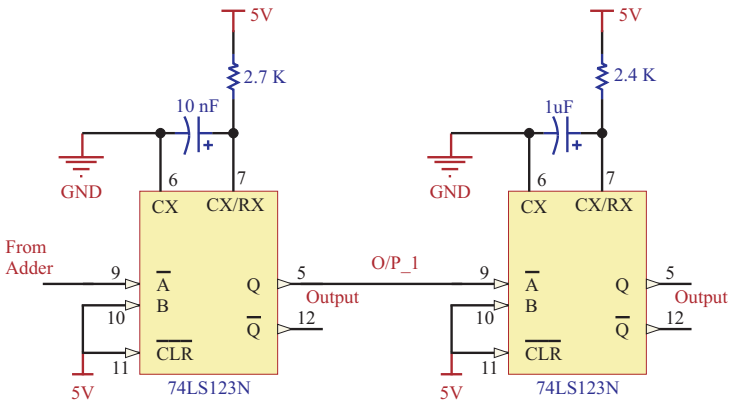


Figure 5.42: Using 74LS123 to generate reinjection pulse $Sp0/Sn0$.

The two reinjection pulses $Sp1/Sn1$ and $Sp2/Sn2$ are added together using a voltage adder circuit with a voltage gain of 2. To maintain a minimum dead-time (10 μs) between $Sp1/Sn1$-$Sp0/Sn0$ and $Sp2/Sn2$-$Sp0/Sn0$ (Fig. 5.42), the falling edge of the added signal is detected

by the 74LS123 and it produces an output pulse for 10 μs wide. C3$_{ext}$ = 0.01 μF and R3$_{ext}$ = 2.7 kΩ. This output from 74LS123 is again fed to 74LS123 which is configured as a falling edge detector and produces an output for 790 μs which takes in account the maximum variation into delay because of component tolerance variation and dead-time. C4$_{ext}$ = 1 μF and R4$_{ext}$ = 2.42 kΩ (Fig. 5.43). The variations in dead-time and pulse width of $Sp0/Sn0$ due to C4$_{ext}$ and R4$_{ext}$ tolerances are listed in the Table 5.8.

Table 5.7: Variation in dead-time due to C3$_{ext}$ and R3$_{ext}$ tolerances.

	Desired	Actual Mean	Actual Min.	Actual Max.	Tolerance
K	0.37	0.37	0.37	0.37	Assumed constant
$R3_{ext}$	2.7 kΩ	2.7 kΩ	2.43 kΩ	2.97 kΩ	10%
$C3_{ext}$	0.01 μF	0.01 μF	0.009 μF	0.011 μF	10%
t_{dead}	10 μs	10 μs	8.09 μs	12 μs	–

Table 5.8: Variation in pulse width of Sp0/Sn0 due to C4$_{ext}$ and R4$_{ext}$ tolerances.

	Desired	Actual Mean	Actual Min.	Actual Max.	Tolerance
K	0.33	0.33	0.33	0.33	Assumed constant
$R4_{ext}$	2.39 kΩ	2.4 kΩ	2.37 kΩ	2.42 kΩ	1%
$C4_{ext}$	1 μF	1 μF	0.99 μF	1.01 μF	1%
t_w	790 μs	792 μs	774 μs	806 μs	–
Width	14.2°	14.25°	14°	14.5°	–

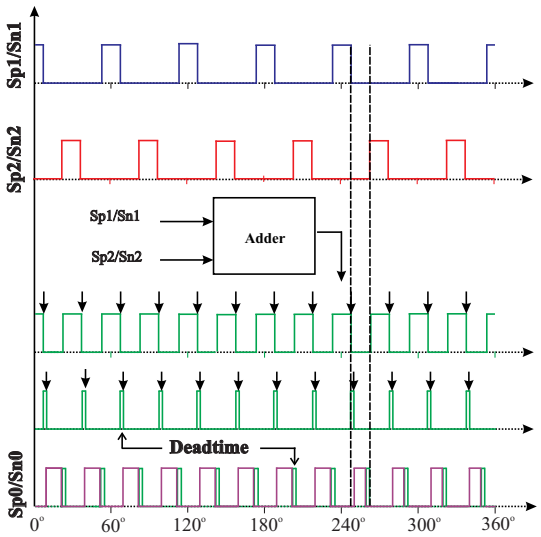


Figure 5.43: Generation of reinjection pulse for reinjection IGBT $Sp0/Sn0$.

The reinjection pulses $Sp1/Sn1$, $Sp0/Sn0$ and $Sp2/Sn2$ are shown in Fig. 5.44, which has a measured dead-time of 12 μs between them. The fabricated 3-level reinjection PCB is shown in Fig. 5.45.

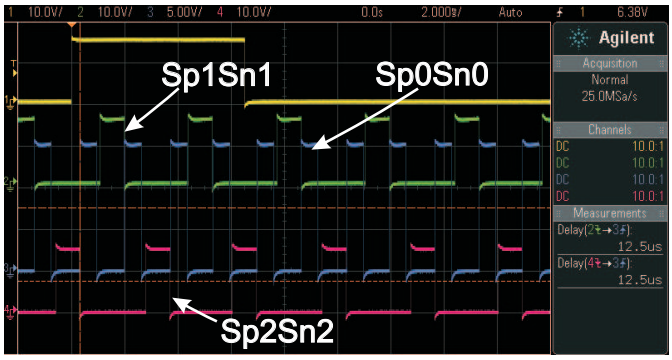


Figure 5.44: Reinjection pulses $Sp1/Sn1$, $Sp0/Sn0$ and $Sp2/Sn2$.

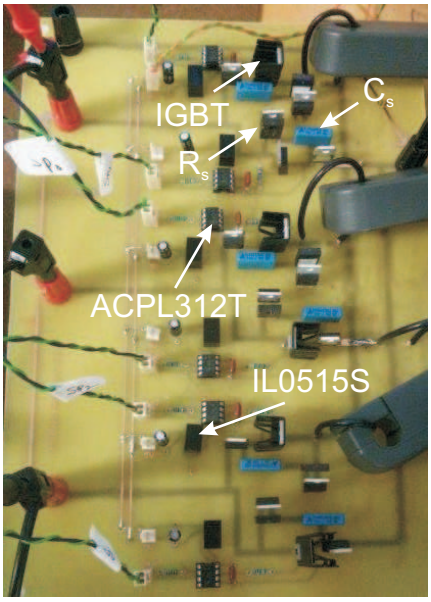


Figure 5.45: The 3-level reinjection PCB, $C_{sn} = 0.01\ \mu$F.

5.8 REINJECTION TRANSFORMER TESTING

The operating frequency of the reinjection transformer, $f_{reinj} = 300$ Hz. The phase voltage RMS rating of the transformer is derived from Fig. 5.46. From Fig. 5.46, the voltage appearing across the primary-side (and secondary-side) of the reinjection transformer (Fig. 5.47) is:

$$\begin{aligned} V_{d_{ac}} &= |V_d - V_{d_{dc}}| \\ &= |\frac{\sqrt{3}V_{pk}}{k_n}\cos(\omega t + \alpha - \frac{\pi}{6}) - \frac{3\sqrt{3}V_{pk}}{k_n \pi}\cos(\alpha)|, \text{ for } 0 \leq \omega t \leq \frac{\pi}{3}, \alpha = -45^\circ \\ &= 0.72\frac{V_{pk}}{k_n}, \text{ maximum voltage across primary} \end{aligned} \tag{5.29}$$

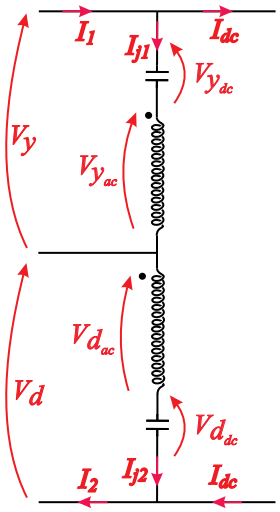


Figure 5.46: Reinjection transformer AC-side voltage derivation.

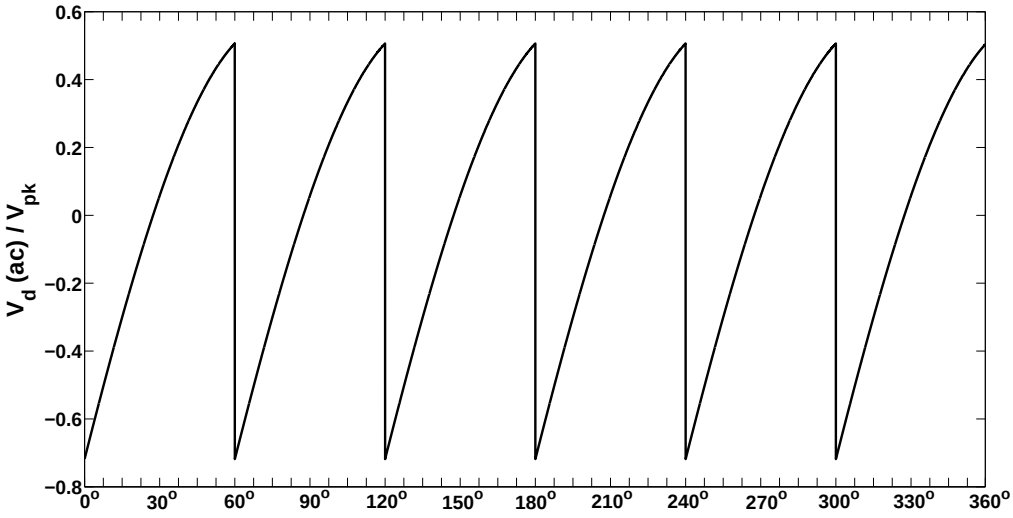


Figure 5.47: Reinjection transformer AC-side voltage waveform for α = -45°.

The RMS current rating of the primary (I_{j1}/I_{j2}) and secondary (I_{s1}/I_{s2}) windings of the reinjection transformer is calculated from Fig. 4.19(d):

$$I_{j_{rms}} = \sqrt{\frac{1}{\pi/6}\left(\int_{0}^{\pi/24} I_{dc}^2 \cdot d\theta + \int_{\pi/8}^{\pi/6} (-I_{dc})^2 \cdot d\theta\right)}$$
$$= 0.707 \times I_{dc} \tag{5.30}$$

The RMS current rating of the primary and secondary winding of the reinjection transformer = $0.707 I_{dc}$ for a 3-level MLCR CSC. Hence, for α = -45°, $V_{dc} \approx$ 97.6 V, $I_{dc} \approx$ 0.97 A, reinjection

transformer rating ≈ 70.41 V/0.68 A. A 1 kVA /400 V (1:1) transformer is used as a reinjection transformer with full-load current = 2.5 A. This overrated transformer is used to take into account any transient conditions that may lead to larger voltages. The following tests are carried out to determine an equivalent circuit of the reinjection transformer. Fig. 5.48 shows the reinjection transformer schematic symbol, and the corresponding commonly used Steinmetz model is shown in Fig. 5.49 where the model voltage and current are defined as V_1: Primary side voltage (V), V_2': Secondary side voltage referred to primary (V) = $\left(\frac{n_1}{n_2}\right) V_2$, I_1: Primary side current (A), I_2': Secondary side current referred to primary (A) = $\left(\frac{n_1}{n_2}\right) I_2$ and I_m: Magnetising current (A).

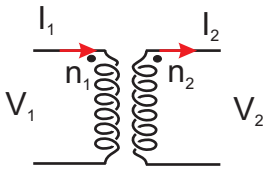


Figure 5.48: Reinjection transformer symbol.

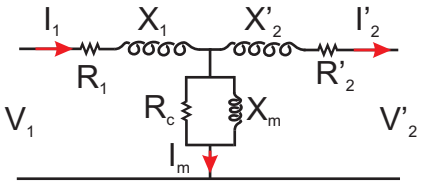


Figure 5.49: Steinmetz model.

The model parameters are: R_1: Primary coil resistance (Ω), X_1: Primary coil reactance (H), R_c: Core loss resistance (Ω), X_m: Core loss reactance (Ω), R_2': Secondary coil resistance referred to primary(Ω) = $\left(\frac{n_1}{n_2}\right)^2 R_2 = R_2$,$X_2'$: Secondary coil reactance referred to primary (Ω) = $\left(\frac{n_1}{n_2}\right)^2 X_2 = X_2$.

5.8.1 DC Resistance Test

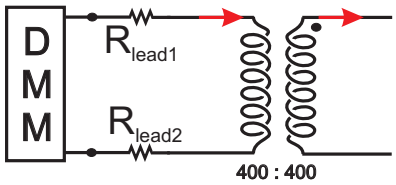


Figure 5.50: Steinmetz model for DC resistance test.

In this test, the resistance parameters R_1 and R_2 are measured using a digital multi-meter (DMM) with correction for lead resistance: R_{leads} = 0.17 Ω. The measured R_1 = 2.01 Ω - 0.17 Ω = 1.84 Ω while R_2 = 2.11 Ω - 0.17 Ω = 1.94 Ω. Hence, R_{eq} = 3.78 Ω.

5.8.2 Short Circuit Test

In this test, the secondary-side of the transformer is short-circuited; the magnetizing current (I_m) is negligible and the equivalent circuit can be approximated as shown in Fig. 5.51. The

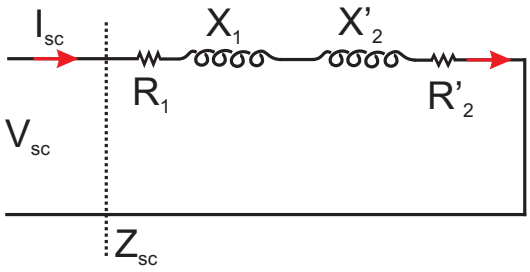


Figure 5.51: Steinmetz model for SC test.

magnetizing impedance is assumed to be much larger than the secondary resistance and secondary leakage reactance. The measured voltage, current and power on the primary side of the transformer are:

Table 5.9: Short-Circuit test results.

Primary voltage V_{sc}	9.92 V
Primary current I_{sc}	2.5 A
Primary power P_{sc}	23.5 W

The transformer parameters are calculated as:

$$R_{eq} = R_1 + R_2' = R_1 + R_2 = \frac{P_{sc}}{{I_{sc}}^2} = \frac{23.5}{2.5^2} = 3.76\ \Omega.$$
$$Z_{eq} = Z_1 + Z_2' = Z_1 + Z_2 = \frac{V_{sc}}{I_{sc}} = \frac{9.92}{2.5} = 3.96\ \Omega$$
$$X_{eq} = X_1 + X_2' = X_1 + X_2 = \sqrt{{Z_{eq}}^2 - {R_{eq}}^2} = \sqrt{3.96^2 - 3.76^2} = 1.242\ \Omega$$

If it is assumed that $X_1 = X_2$, then $X_1 = X_2 = 0.621\ \Omega$.

5.8.3 Open Circuit Test

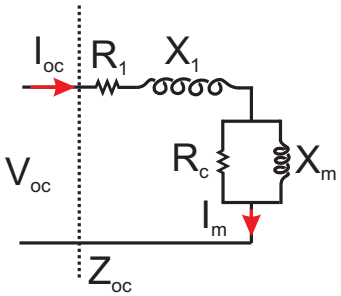


Figure 5.52: Steinmetz model for OC test.

The next test involves open-circuiting the secondary-side of the reinjection transformer and applying rated voltage to the primary-side. Under this condition, the Steinmetz equivalent circuit reduces to that shown in Fig. 5.52. The measured voltage, current and power on the primary side of the transformer are:

Table 5.10: Open-Circuit test results.

Primary voltage V_{oc}	300 V (Maximum AC voltage available from Chroma 61504)
Primary current I_{oc}	0.104 A
Primary power P_{oc}	16 W

The power factor is determined as:

$$\cos\phi = \frac{P_{oc}}{V_{oc}I_{oc}} = \frac{16}{300 \times 0.104} = 0.512$$

$$R_c = \frac{V_{oc}}{I_{oc}\cos(\phi)} = \frac{300}{0.104 \times 0.512} = 5\ \text{k}\Omega$$

$$X_m = \frac{V_{oc}}{I_{oc}\sin(\phi)} = \frac{300}{0.104 \times 0.858} = 3.36\ \text{k}\Omega$$

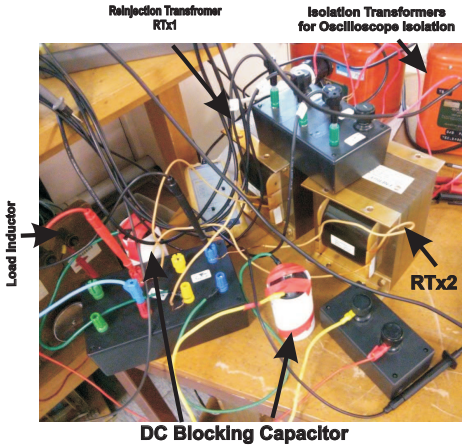


Figure 5.53: The reinjection transformer and DC blocking capacitor.

5.9 DC BLOCKING CAPACITOR

From Eqn. 5.29, the maximum steady-state DC voltage appearing across the DC blocking capacitor is $\frac{3\sqrt{3}V_{pk}}{k_n\pi} = \frac{3\sqrt{3}\cdot 325.27}{8\pi} = 67.25$ V. A 400 V/ 1 mF (PEH200 Series, ±20%) electrolytic capacitor is used as the DC blocking capacitor. From Eqn. 4.20, the maximum $V_{dc} \approx 138$ V, I_{dc} = 1.4 A. The maximum RMS value of reinjection currents I_{j1} and I_{j2} = 0.707× 1.4 A = 0.989 A ≈ 1 A.

For an electrolytic capacitor, the 'Impedance' is calculated:

$$Z = \sqrt{R_s^2 + (X_c^2 - X_L^2)} \tag{5.31}$$

where R_s: Equivalent Series Resistance (ESR), L_s: Equivalent Series Inductance, C: Rated Capacitance. This capacitor is rated for a total of 5.9 A based on an ESR of 76 mΩ at a frequency of 100 Hz and ESL of 16 nH which gives $Z_{100Hz} = 1.59\ \Omega$. Fig. 5.53 shows the set-up for the reinjection transformer along with the DC blocking capacitors.

5.10 CONCLUSIONS

1. The details of TCA785 based FAC for the main bridge of the MLCR CSC are presented. The design of various hardware modules such as transducer circuits, forward-converter based thyristor driver circuit and IGBT driver circuits are detailed.

2. Based on the TCA785 FAC and a forward-converter based thyristor driver circuit, a prototype 12-pulse thyristor converter is tested in the laboratory. Satisfactory results are obtained and use of TCA785 is illustrated.

3. The ability to extend the firing angle range between $-180^\circ \leq \alpha \leq 180^\circ$ using TCA785 is established. Based on the firing signals obtained using this FAC, the firing signals for the reinjection IGBTs are derived. The variation in timing delay and pulse-width due to RC component tolerance variation is considered.

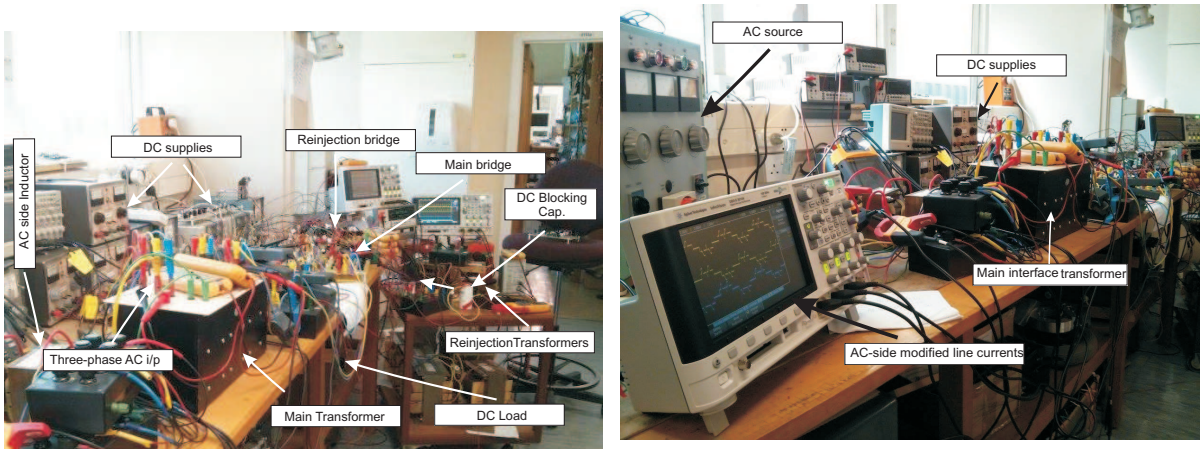
4. The detailed testing of the reinjection transformer is also presented, and the transformer parameters are calculated. The choice of the DC blocking capacitor is also explained.

Chapter 6

TEST RESULTS: 3-LEVEL MLCR CSC

6.1 INTRODUCTION

This chapter presents the first experimental validation of the theoretical and PSCAD/EMTDC model of a 3-level thyristor based MLCR CSC. For this purpose, a prototype (the set-up is shown in Fig. 6.1) is tested in the laboratory. The rest of the chapter is organised as follows: Section 6.2 presents the theoretical and PSCAD/EMTDC results along the experimental results, Section 6.3 presents the modification of current waveforms due to a 'very large' snubber capacitor C_{sn}.

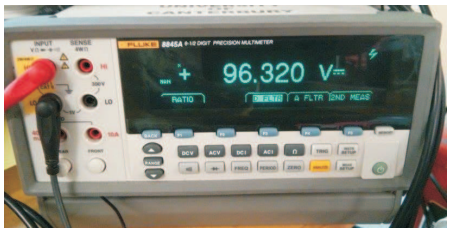


(a): The laboratory set-up for the MLCR CSC. (b): AC-side modified line currents in MLCR CSC.

Figure 6.1: MLCR CSC laboratory prototype.

6.2 PSCAD/EMTDC SIMULATION AND EXPERIMENTAL RESULTS

The average theoretical V_{dc} for a 3-level MLCR CSC with α = -45° is (Eqn. 4.20): 97.6 V and the average theoretical I_{dc} is: 0.97 A. Figs. 6.2(a)-6.2(b) shows the experimental V_{dc} = 96.32 V and measured I_{dc} = 0.94 A obtained from the prototype.

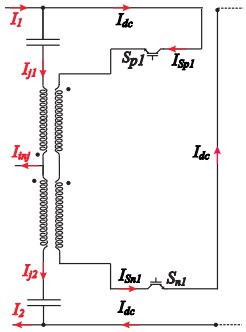


(a): Measured V_{dc} for MLCR prototype.

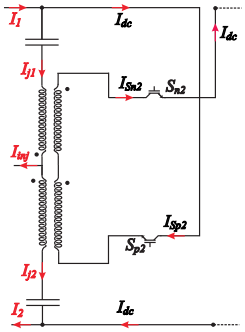
(b): Measured I_{dc} for MLCR prototype.

Figure 6.2: Measured V_{dc} and I_{dc} obtained from MLCR CSC prototype.

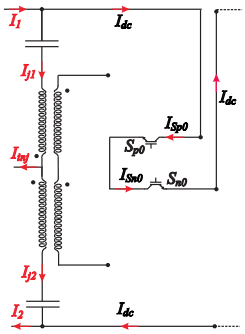
6.2.1 Formation of I_{inj} using reinjection bridge



(a): Reinjection bridge current: S_{p1}/ S_{n1} are on.



(b): Reinjection bridge current: S_{p2}/ S_{n2} are on.



(c): Reinjection bridge current: S_{p0}/ S_{n0} are on.

Figure 6.3: Operation of the 3-level reinjection bridge.

For comparison with the ideal waveforms, the ideal and experimental current waveforms are overlapped together. Steady-state waveforms for α = -45° and snubber components R_{sn} = 1 kΩ and C_{sn} = 0.01 μF are presented in this section. The snubber components used are:

- C_{sn} 0.01 μF, EPCOS - B32652 Series, ± 5%, 1 kV, Polypropylene capacitor.

- R_{sn} 1 kΩ, VISHAY - LTO 30 Series, ± 5%, Ceramic resistor.
- D_{sn} STTH3010D, STMICROELECTRONICS, 1 kV, Fast Recovery diode.

The formation of the 3-level injection current I_{inj}, is shown in Fig. 6.3. I_{inj} is composed of I_{j1} and I_{j2}, in the primary-side of the reinjection transformer. The connection of the reinjection transformer allows the addition of I_{j1} and I_{j2} to form I_{inj}. I_{inj}, with frequency six times the fundamental, is injected into the mid point of the Y-Y and Y-D connected bridges. $I_{j1} = I_{dc}$ when reinjection switch pair S_{p1}/S_{n1} is ON and I_{j1} = -I_{dc} when reinjection switch pair S_{p2}/S_{n2} conducts. When S_{p0}/S_{n0} pair is conducting, the zero-level is obtained and reinjection bridge is bypassed.

Fig. 6.5 shows the currents flowing through the reinjection IGBTs S_{p1}, S_{p0} and S_{p2}. The PSCAD/EMTDC results (here, the ideal waveforms are normalised to I_{dc} obtained from simulation) are shown in Fig. 6.5(a), whereas the experimental waveforms are shown in Fig. 6.5(b). The switching pattern of the reinjection IGBTs constitute the "chopping" of I_{dc} to form a 3-level AC waveform in the secondary windings of the reinjection transformer. A close match between PSCAD/EMTDC results (Fig. 6.6(a)) and experimental results (Fig. 6.6(b)) can be seen and the I_{inj} current follows the theoretical waveform. The experimental current waveforms are slightly distorted when compared to the theoretical waveforms. This is due to the RC snubber across the reinjection IGBT switches. The effect of RC snubber circuit was not considered while deriving the theoretical waveforms.

6.2.2 Formation of Stepped DC bus currents

The 3-level injection current I_{inj} combines with I_{dc} to shape the DC bus currents I_1 and I_2 into a three-level waveform as shown in Fig. 6.7. The PSCAD/EMTDC results are shown in Fig. 6.7(a) and experimental waveforms are presented in Fig. 6.7(b). The reinjection switching strategy ensures I_1 and I_2 are zero during main bridge commutation instants, i.e. 0°, 30°, 60°, 90°, 120°, 150°, 180°, 210°, 240°, 270°, 300°, 330° and 360°.

6.2.3 Modification of AC-side currents due to I_1 and I_2

The PSCAD/EMTDC results for the AC-side line current waveforms I_{aY} and I_{caD} in the secondary-side of the interface transformer are shown in Fig. 6.8(a). *In the experimental set-up, current I_{caD} is not available for measurement*, hence the line current I_{aD} is shown in Fig. 6.8(b) instead. Experimental line current I_a follows the theoretical waveform and a 24-step primary-side line current I_a is obtained. This shows that the MLCR concept transforms the conventional line current waveform into a multi-step AC current waveform i.e a 12-step waveform has been

transformed into a 24-step waveform with the help of the I_{inj} which in turn modifies I_{aY} and I_{caD}. This confirms the theory that line current THD reduction is possible by 3-level current reinjection.

6.2.4 Modified main bridge thyristor current waveform

The modified current (I_{thyY1}) through thyristor Y1 is shown in Fig. 6.9. The PSCAD/EMTDC result (Fig. 6.9(a)) is a very close match to the theoretical analysis, whereas the experimental current (Fig. 6.9(b)) also follows the theoretical wave-shape fairly accurately. It is seen from Fig. 6.9(b) that I_{thyY1} does not begin to flow at the instant when thyristor Y1 is fired but at the instant determined by the auxiliary reinjection bridge. Thus, current flow through thyristor can be controlled independently using the reinjection bridge. This demonstrates the ability to operate thyristors as self-commutated switches and with a negative firing angle.

6.2.5 Voltage waveforms

The DC-side voltage waveforms are time referenced with respect to the AC-side current waveform I_a (Fig. 6.8). This is done to show that even with thyristor based converter, it is possible to switch the thyristors with a negative firing angle. Again for comparison with the ideal waveforms, the theoretical and experimental voltage waveforms are overlapped together. Fig. 6.10(a) shows the PSCAD/EMTDC waveforms for the DC voltages V_y and V_d obtained from the Y-Y and Y-D connected bridges. These waveforms show voltage spikes which start exactly 7.5° before and after the ideal waveform switching instant, which are capped around 180 V due to the snubber capacitor $C_{sn} = 0.01$ μF. This voltage spike in PSCAD/EMTDC can be reduced by using a larger snubber capacitor C_{sn}. Fig. 6.10(b) shows the experimental V_y and V_d where such a spike is not seen. A clear difference in PSCAD/EMTDC and experimental results is observed. Fig. 6.11 shows the 12-pulse DC bus voltage V_x is actually the sum of V_y and V_d.

The 6-pulse DC bus voltage V_y and DC component of V_y voltage: $V_y(dc)$ across the DC blocking capacitor is shown in Fig. 6.12. Because of the voltage spike in PSCAD/EMTDC, $V_y(dc)$ is higher than the theoretical $V_y(dc)$. The experimental $V_y(dc)$ is very close to theoretical value as seen in Fig. 6.12(b). Fig. 6.13 shows the measured ripple voltage across the DC blocking capacitor. With C = 1 mF, a ripple voltage of 1.3 V is obtained in this set-up.

Fig. 6.14 shows the AC component of V_y and V_d across the reinjection transformer's primary and secondary windings. The reverse-connected reinjection transformer across the Y-Y connected bridge allows secondary-side $V_y(ac)$ to be opposite to that of primary-side $V_y(ac)$.

The reinjection transformer secondary-side voltage V_m is shown in Fig. 6.15. However, the $\frac{dv}{dt}$ voltage spike (starting exactly 7.5° before and after the ideal waveform switching instant) seen

in the PSCAD/EMTDC waveforms in V_y and V_d is reflected into V_m (Fig. 6.15(a)). Voltage spikes $\geq \pm 200$ V is seen in the PSCAD/EMTDC waveforms. In Fig. 6.15(b), experimental V_m follows the theoretical wave-shape but spikes (of ± 40 V) are observed around each commutation instant. The transition delay observed in the PSCAD/EMTDC waveform is not seen in the experimental waveform.

Based on a reinjection switching pair, reinjection voltage V_z (Fig. 6.16), is obtained from V_m. The PSCAD/EMTDC waveform does not follow the theoretical waveform as seen in Fig. 6.16(a) whereas the experimental waveform is following the theoretical waveform with voltage spikes observed at 60°, 120°, etc commutation instants. The DC-side voltage ripple is transferred via the reinjection transformer, shifted by the 3-level reinjection bridge as V_z and it gets added to V_x, which increases the DC-side voltage waveform pulse number by a factor of two. The output DC voltage V_{dc} is shown in Fig. 6.17. The experimental V_{dc} (Fig. 6.17(b)) shows the distortion which appears across V_z at 60°, 120°, etc commutation instants. Nevertheless, 24-pulses are obtained on V_{dc} which implies the reinjection voltage V_z is getting added to the 12-pulse DC bus voltage V_x to form 24-pulse V_{dc}. The multi-pulse DC voltage waveform is experimentally verified.

6.3 MODIFICATION OF CURRENT WAVEFORMS DUE TO 'VERY LARGE' C_{SN}

To investigate the effect of using a large snubber capacitor C_{sn}, the 0.0l μF capacitor was replaced with a l μF (WIMA - MKP4 Series, $\pm 10\%$ Polypropylene) capacitor. The 3-level reinjection PCB with $C_{sn} = 1$ μF is shown in Fig. 6.4.

The effect of changing the C_{sn} can be clearly observed in Fig. 6.18. The current waveforms through the reinjection IGBTs have a slower $\frac{di}{dt}$ with respect to a smaller C_{sn}. The experimental current waveforms I_{Sp1} and I_{Sp2} (Fig. 6.18(b)) are equal to I_{dc} only for half the theoretical duration. The effect of this slow $\frac{di}{dt}$ can be seen on the reinjected current I_{inj} (Fig. 6.19(b)) where the experimental waveform does not follow the theoretical I_{inj}.

Similarly, the DC bus currents I_1 and I_2, although having a 3-level step, do not follow the theoretical waveform properly as seen in Fig. 6.20. The effect of this inaccurate DC bus current shaping can be seen clearly on I_a, the AC-side line current waveform (Fig. 6.21). In this case, additional current spikes can be observed in I_{aY} and I_{aD} (Fig. 6.21(a)), which are clearly reflected to the primary side current I_a. Although I_a follows the theoretical current wave-shape, its shape is highly distorted with a measured THD of 22.3%. Clearly, the effect of a 'very large' snubber capacitor is to distort the line current highly and the use of a large C_{sn} is not recommended.

The transitions in V_y and V_d are delayed by 7.5° (Fig. 6.22(a)), similar to PSCAD/EMTDC

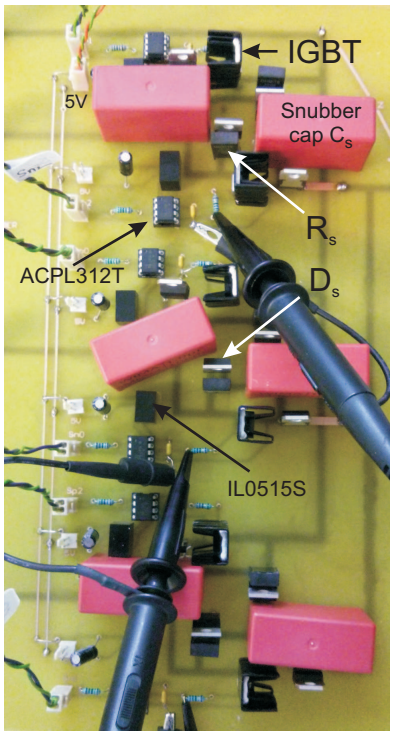


Figure 6.4: The 3-level reinjection PCB with $C_{sn} = 1$ μF.

results. The output DC voltage V_{dc} with $C_{sn} = 1$ μF is shown in Fig. 6.22(d). The voltage spikes in V_{dc} are reduced with $C_{sn} = 1$ μF as compared to V_{dc} with $C_{sn} = 0.01$ μF. However, a distorted 24-step AC-side current and a 24-pulse DC-side voltage is also confirmed with $C_{sn} = 1$ μF.

6.4 CONCLUSIONS

This chapter provided a detailed comparison between PSCAD/EMTDC and experimental results for a 3-level MLCR CSC. The investigation of the performance of the 3-level MLCR CSC under steady-state conditions showed that line currents were able to follow the theoretical current wave-shape. The technical concerns which have been addressed from the experimental results are:

- The modification of the current through the main bridge thyristor shows that self- commutation can be achieved using the reinjection bridge despite finite turn off-time of thyristors.
- As the reinjection IGBTs can be turned off at will, the main bridge thyristor can be switched on at a negative firing angle. This provides the thyristor main bridge reactive power control capability.
- With the help of the auxiliary reinjection bridge, commutation is avoided/reduced due to cancellation of thyristor current in the commutation instants which eliminates the overlap.

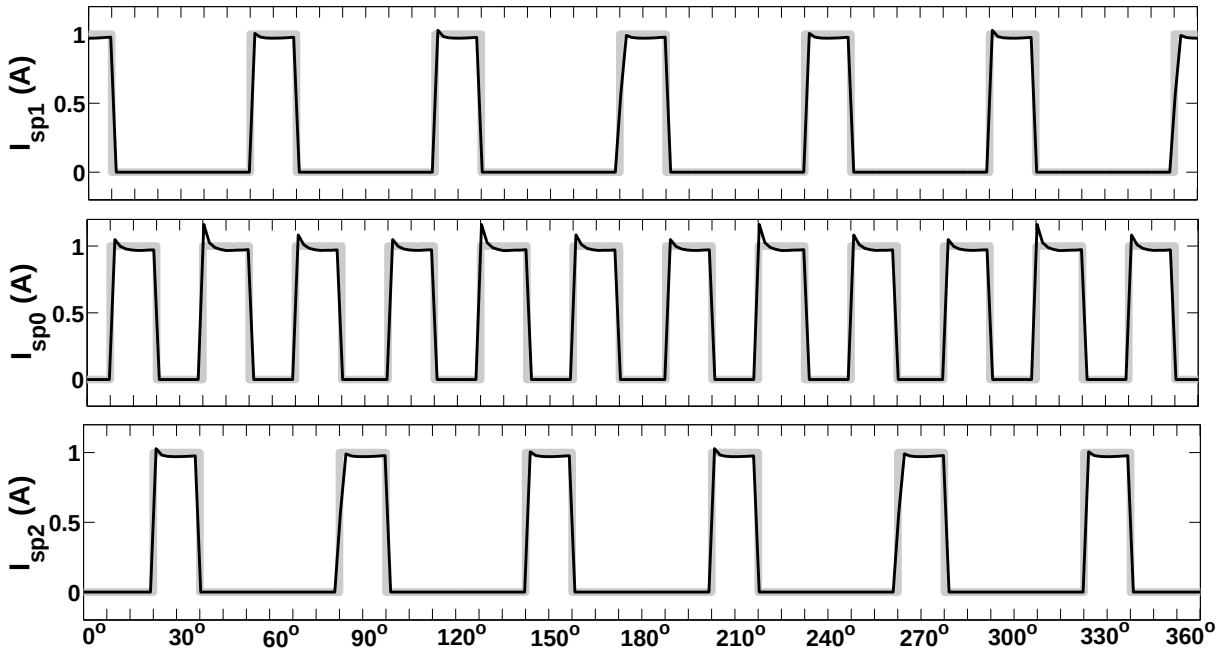
- The DC voltage ripple is transferred via the reinjection transformer and shifted, multiplied and added by the reinjection bridge to the DC voltage increasing output voltage pulse number. The 3-level MLCR concept provides 24-pulse operation of a 12-pulse thyristor converter. Size reduction of the smoothing inductor due to a low harmonic content on the DC-side is possible.

- Size reduction of reinjection transformer is possible due to operation at 300 Hz. These transformers apply a low voltage to reinjection switches.

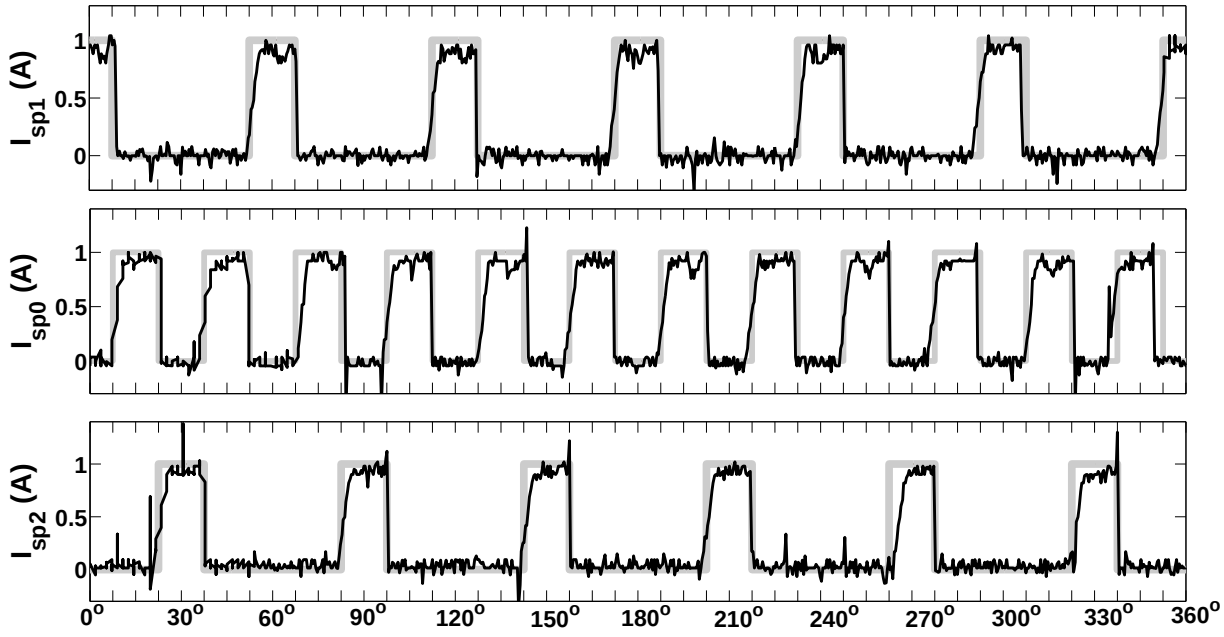
- The 3-level varying DC bus current modifies the AC-side line current, thereby reducing harmonic current distortion caused by thyristor based converters.

- Two RCD snubber capacitors, classified as 'small' and 'very large' are used in the experimental set-up to investigate effect of different snubber components on the performance of the 3-level MLCR CSC. With the 'small' snubber the AC-side current waveforms followed the theoretical wave-shape; whereas with the 'very large' snubber capacitor, the AC-side current waveforms are highly distorted.

- The efficiency of the prototype 3-level MLCR CSC is calculated as:
  Input power $= \frac{3}{\sqrt{2}} V_{pk} I_{a_{RMS}} \cos(\alpha) = \frac{3}{\sqrt{2}} \times 326 \times 0.19 \times \cos(-45) = 92.91$ W,
  Output power $= V_{dc} \times I_{dc} = 96.32 \times 0.94 = 90.54$ W, Efficiency $= 97.45\%$

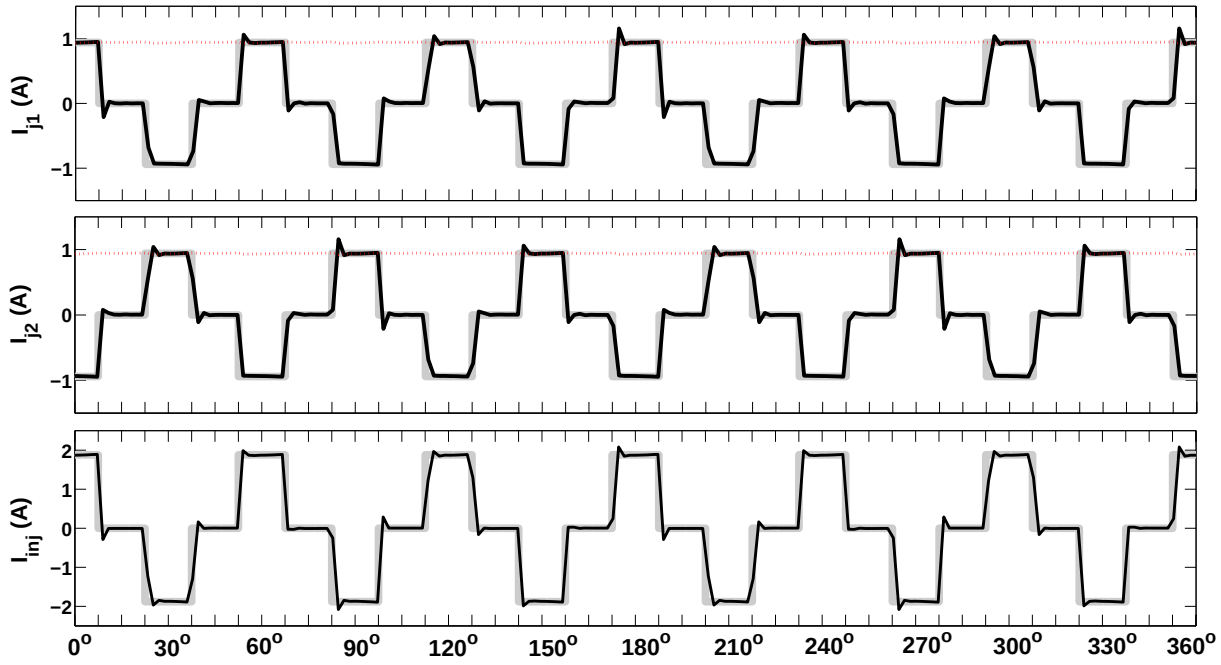


(a): I_{sp1}, I_{sp0} and I_{sp2} **PSCAD/EMTDC** waveforms.

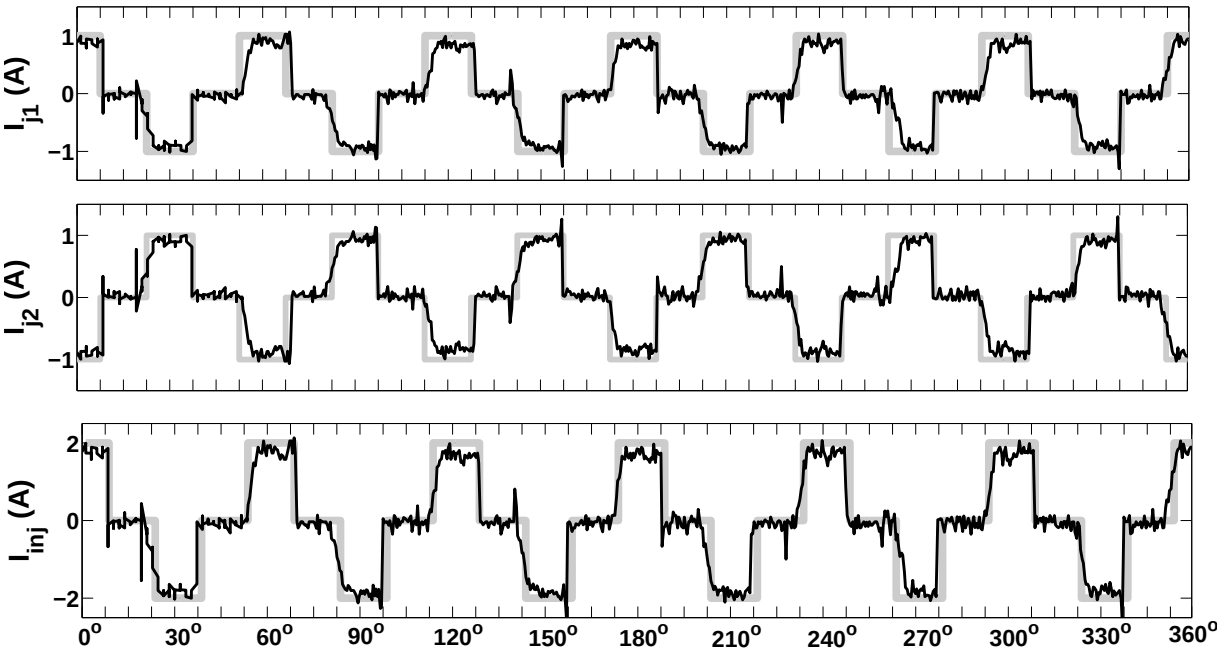


(b): I_{Sp1}, I_{Sp0} and I_{Sp2} **experimental** waveforms, $C_{sn} = 0.01$ μF.

Figure 6.5: Currents through reinjection IGBT with 'small' C_{sn}.

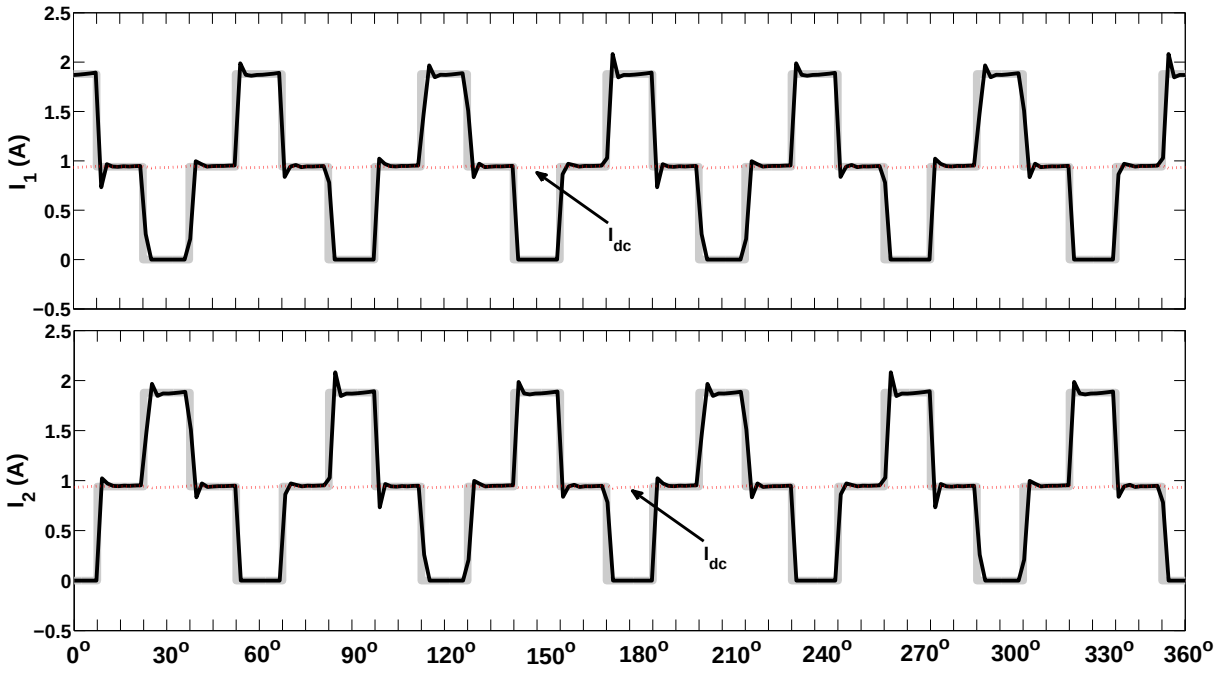


(a): I_{j1}, I_{j2} and I_{inj} **PSCAD/EMTDC** waveforms.

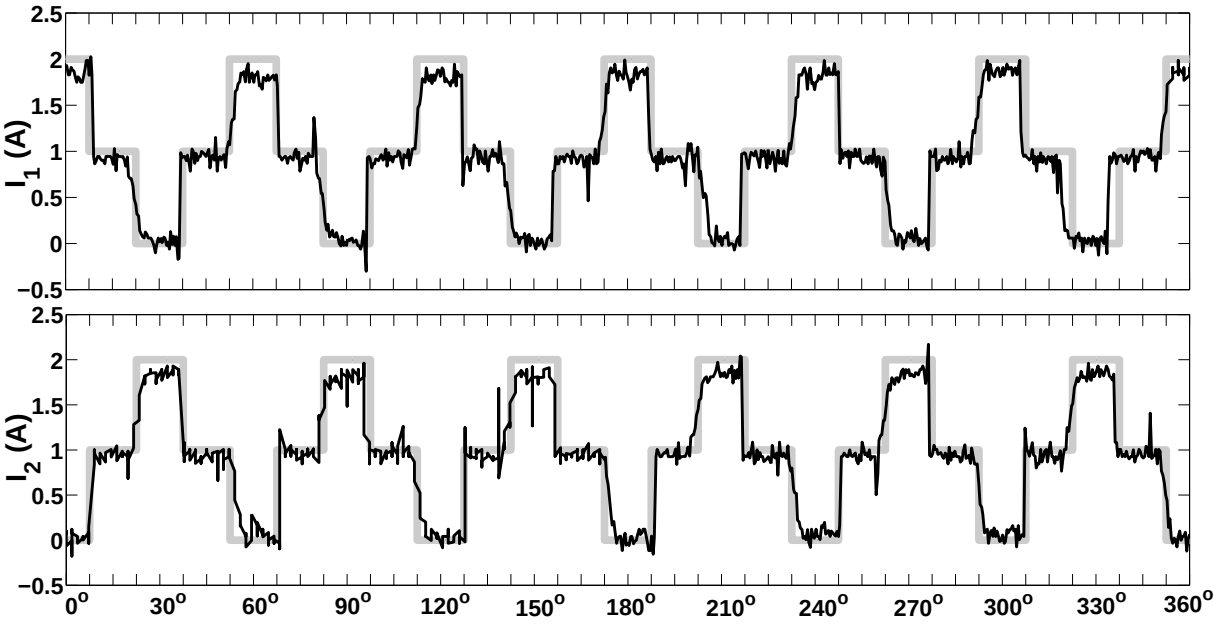


(b): I_{j1}, I_{j2} and I_{inj} **experimental** waveforms, $C_{sn} = 0.01$ μF.

Figure 6.6: Reinjection current waveforms with 'small' C_{sn}.

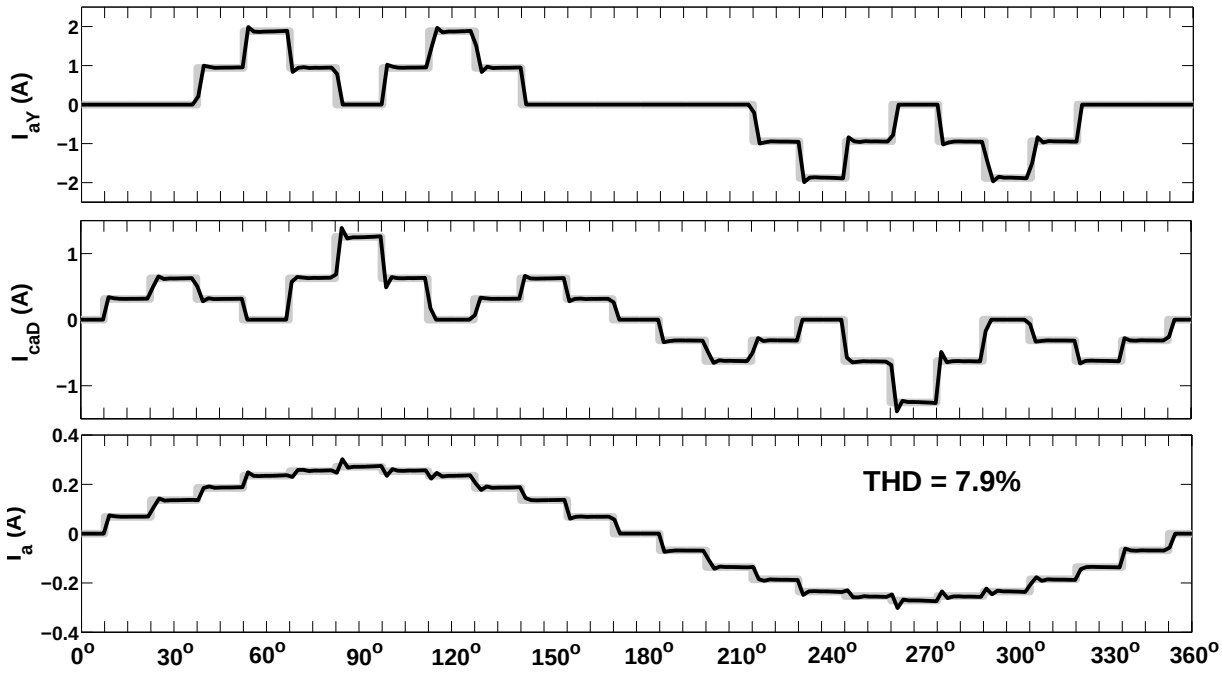


(a): I_1 and I_2 **PSCAD/EMTDC** waveforms.

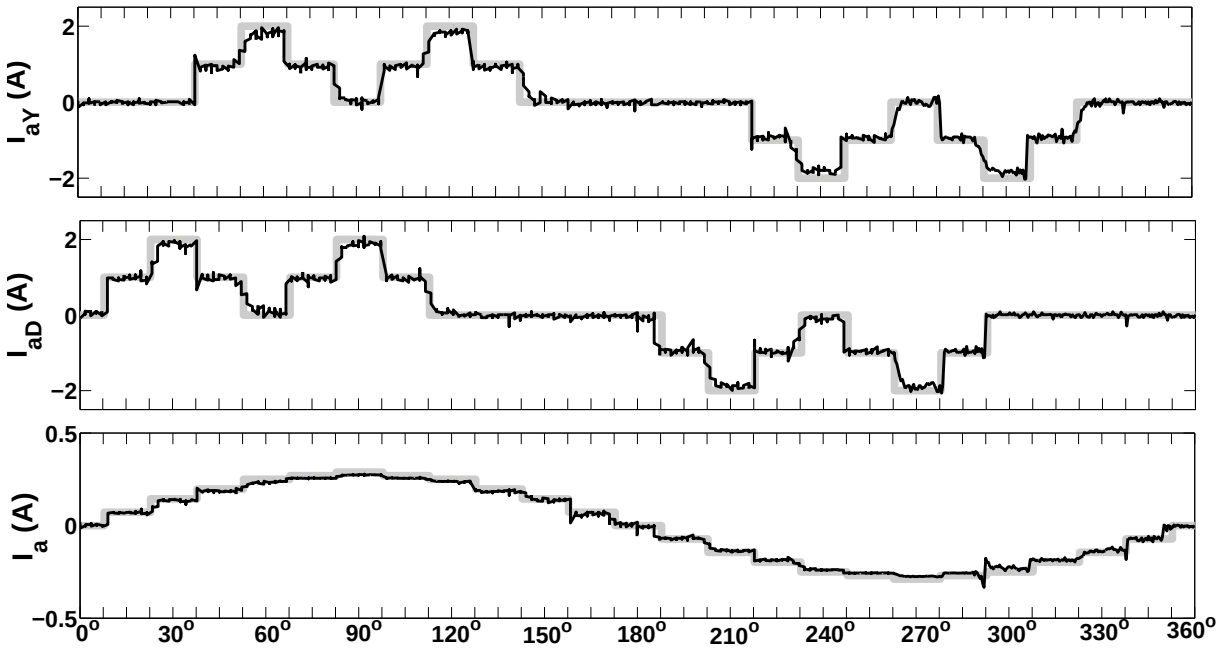


(b): I_1, I_2 **experimental** waveforms, $C_{sn} = 0.01$ μF.

Figure 6.7: DC bus current waveforms with 'small' C_{sn}.

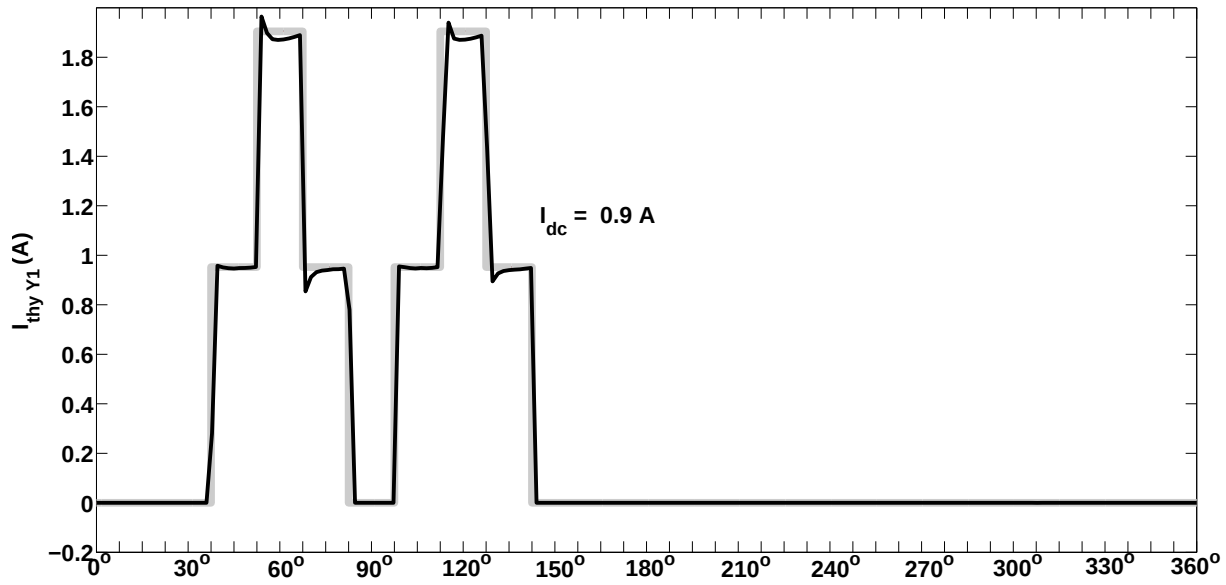


(a): I_{aY}, I_{caD} and I_a **PSCAD/EMTDC** waveforms.

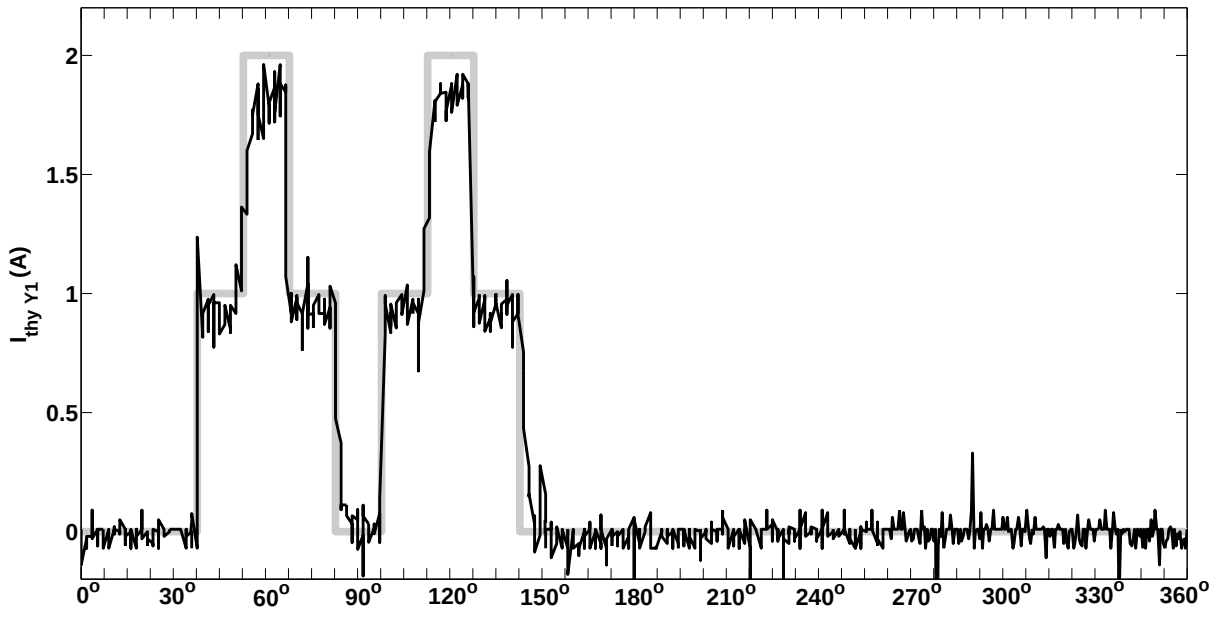


(b): I_{aY}, I_{aD} and I_a **experimental** waveforms, $C_{sn} = 0.01$ μF.

Figure 6.8: AC-side current waveforms with 'small' C_{sn}.

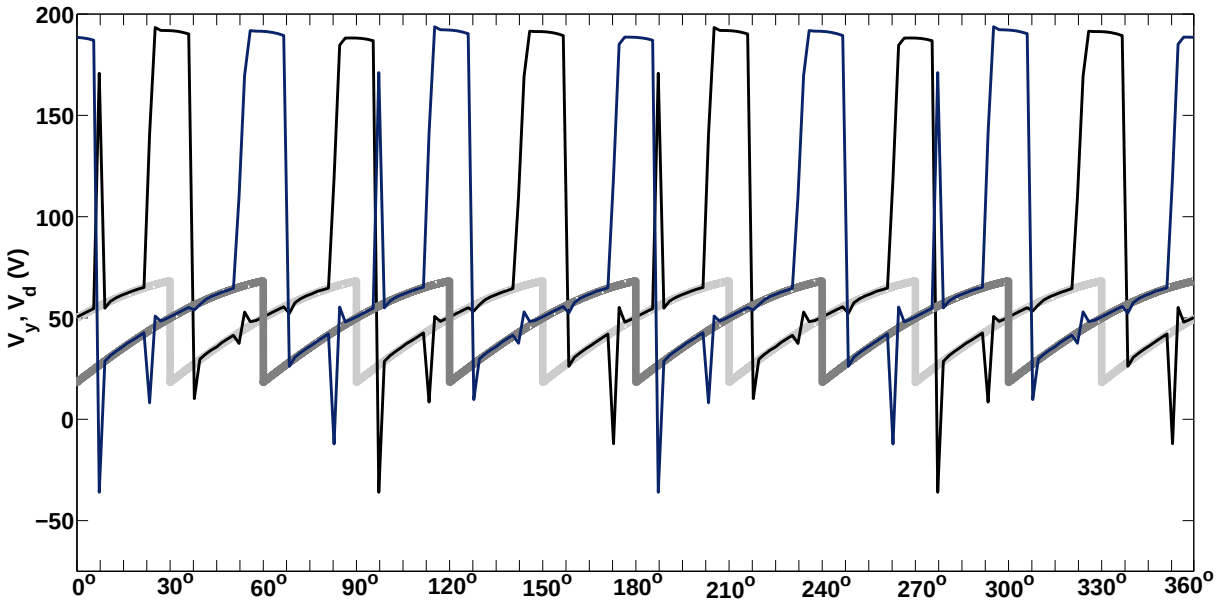


(a): I_{thyY1} **PSCAD/EMTDC** current waveform.

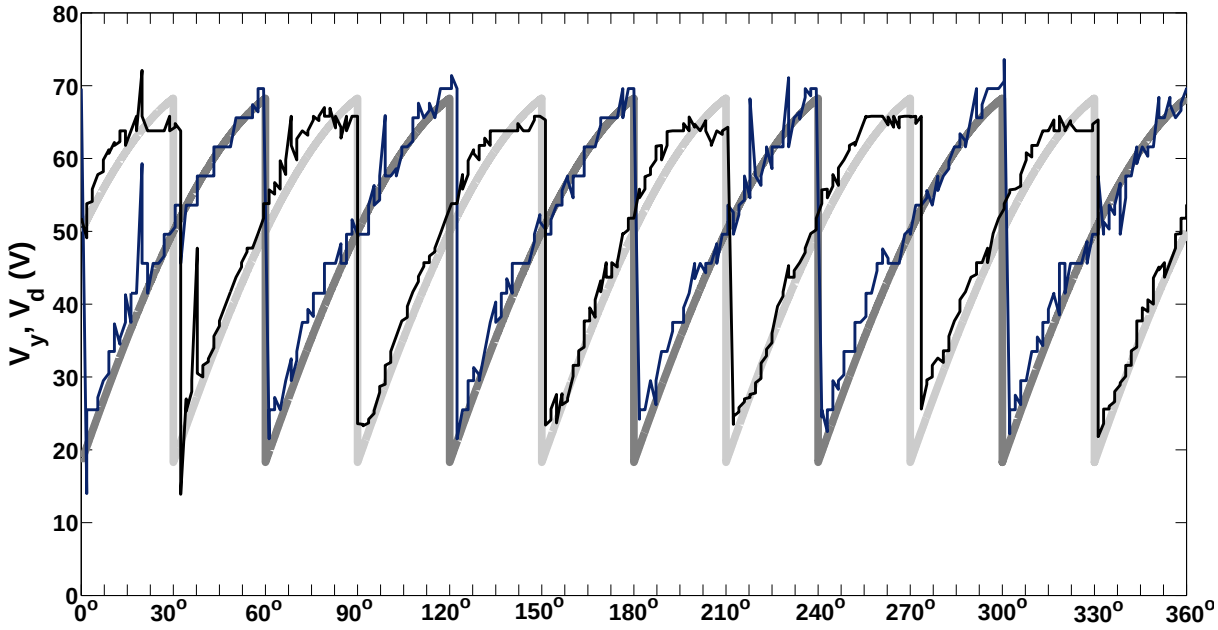


(b): I_{thyY1} **experimental** waveform, $C_{sn} = 0.01$ μF.

Figure 6.9: Current waveform via thyristor Y1 with 'small' C_{sn}.

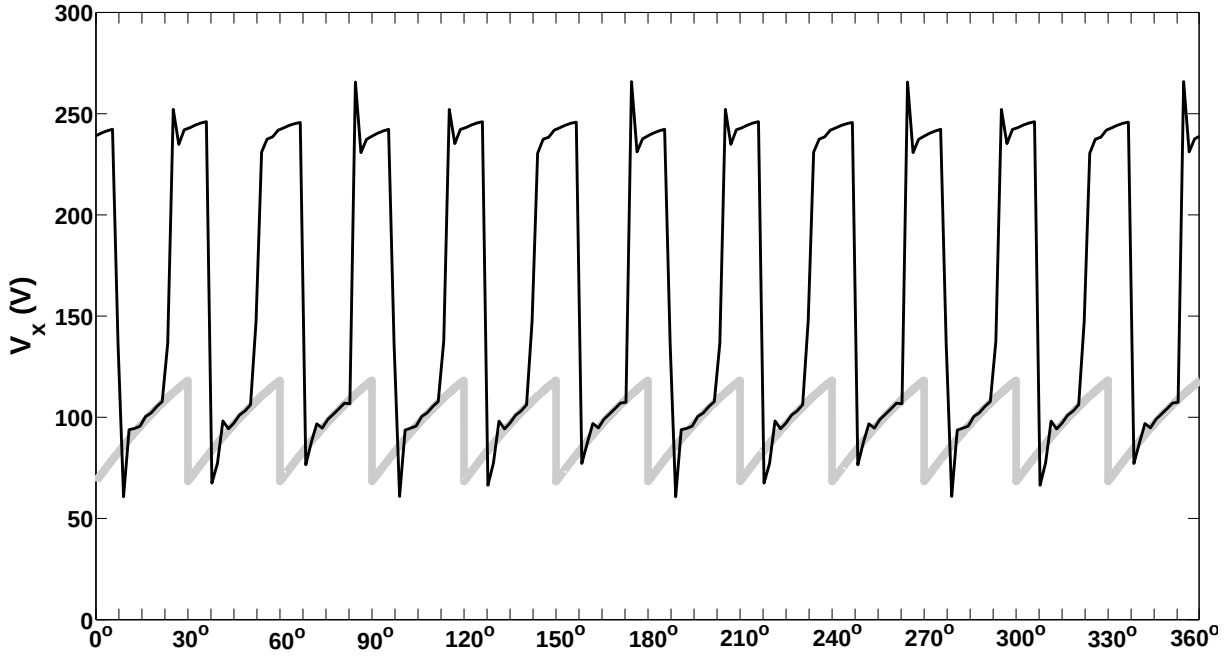


(a): 6-pulse **PSCAD/EMTDC** DC bus voltages V_y and V_d.

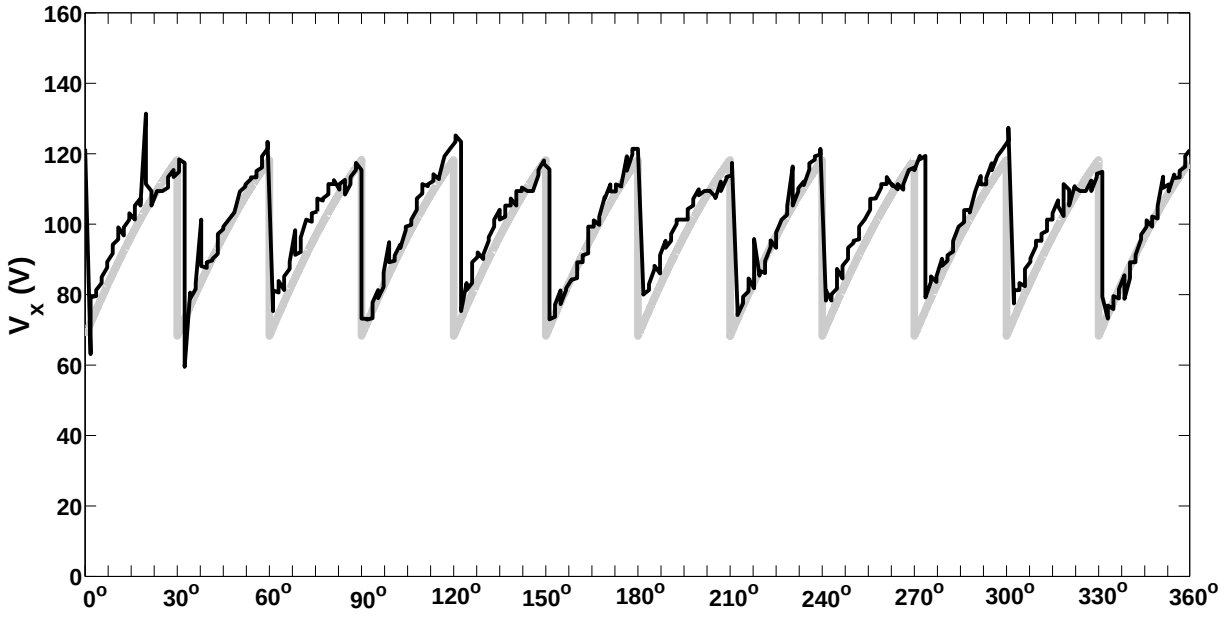


(b): 6-pulse **experimental** DC bus voltages V_y and V_d, $C_{sn} = 0.01$ μF.

Figure 6.10: 6-pulse DC bus voltages V_y and V_d with 'small' C_{sn}.

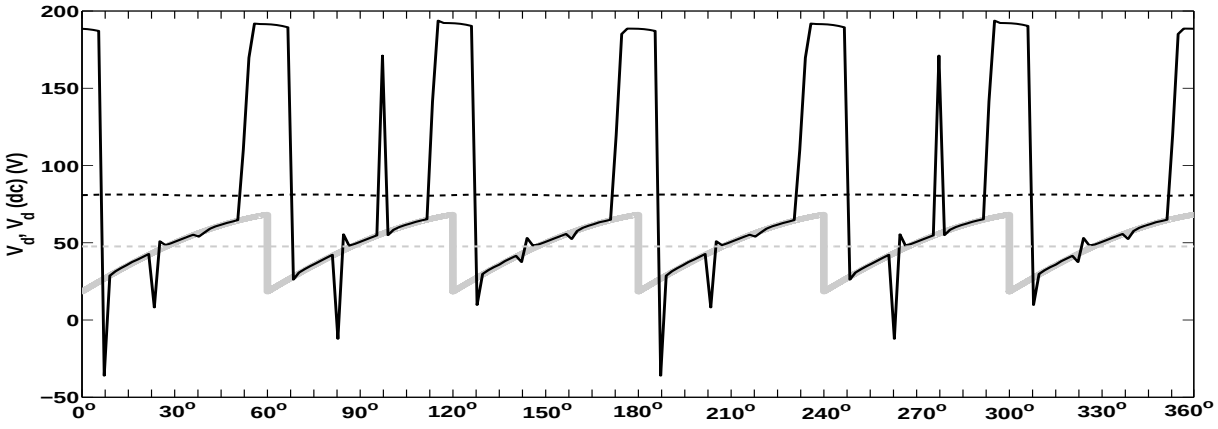


(a): 12-pulse **PSCAD/EMTDC** DC bus voltage V_x.

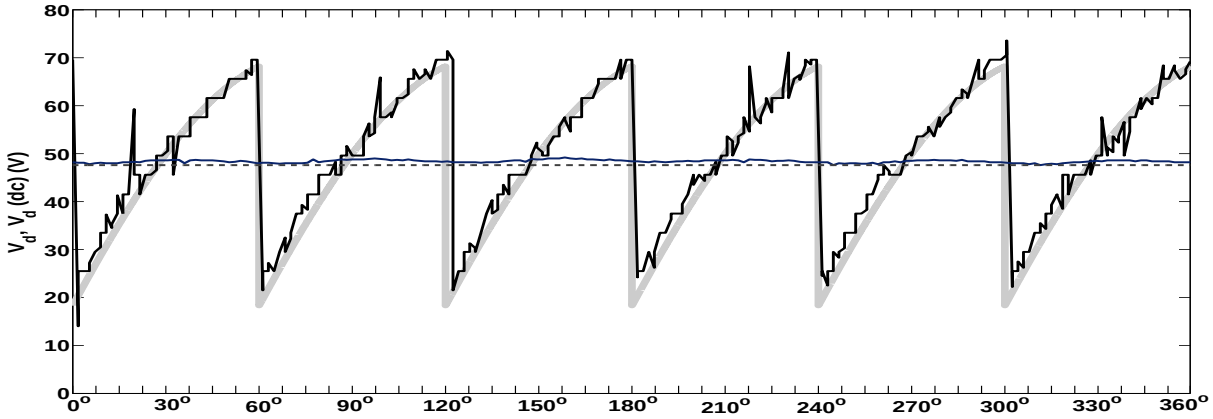


(b): 12-pulse **experimental** DC bus voltage V_x, $C_{sn} = 0.01$ μF.

Figure 6.11: 12-pulse DC bus voltage V_x with 'small' C_{sn}.



(a): 6-pulse **PSCAD/EMTDC** DC bus voltages V_d and DC voltage $V_d(dc)$ across C.



(b): 6-pulse **experimental** DC bus voltages V_d and DC voltage $V_d(dc)$ across C, $C_{sn} = 0.01$ μF.

Figure 6.12: 12-pulse DC bus voltage V_x with 'small' C_{sn}.

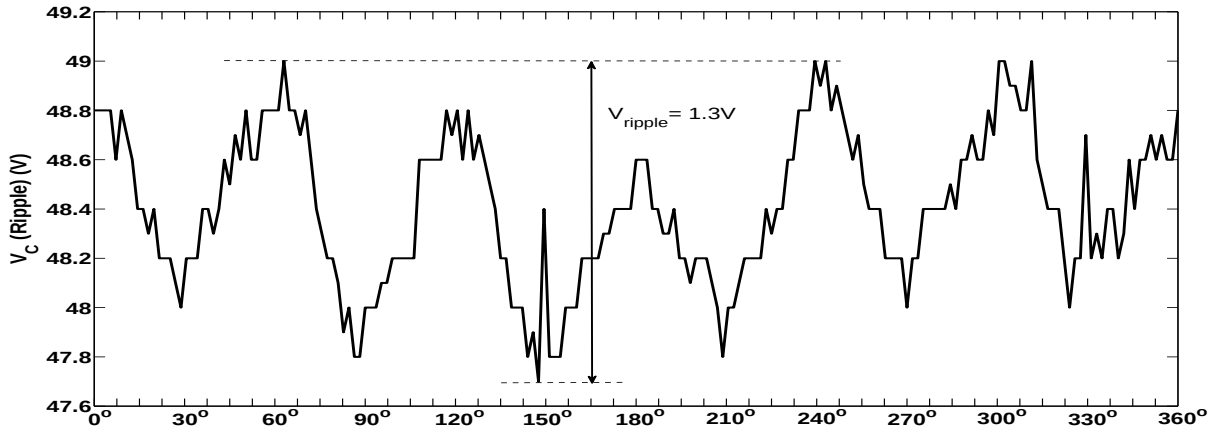
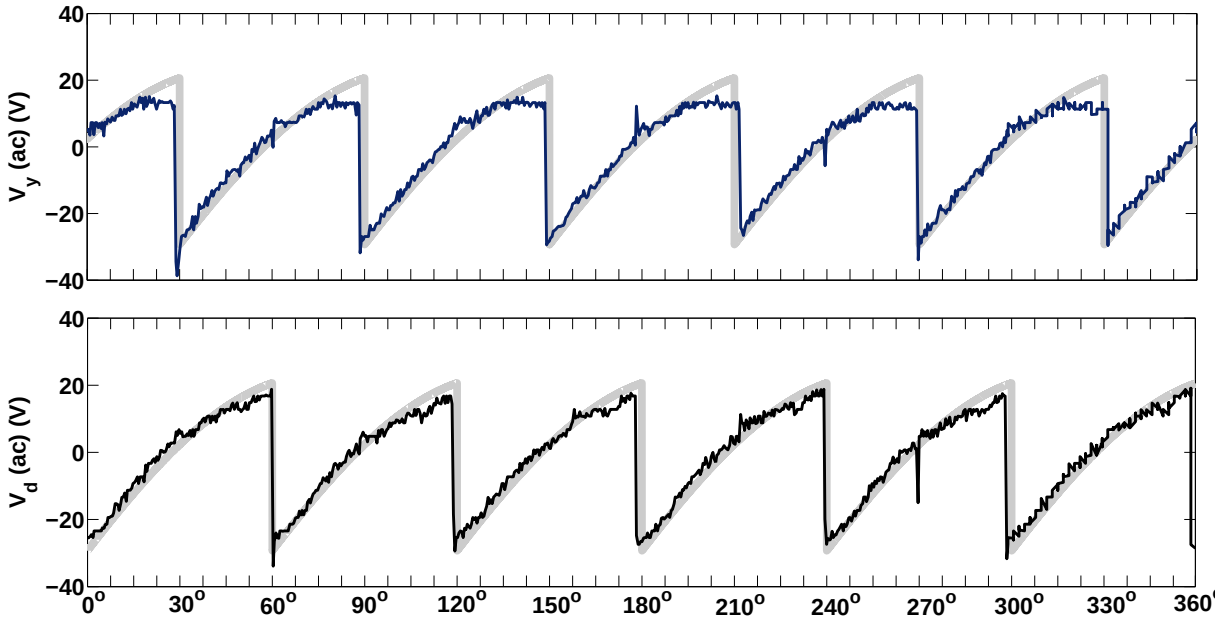
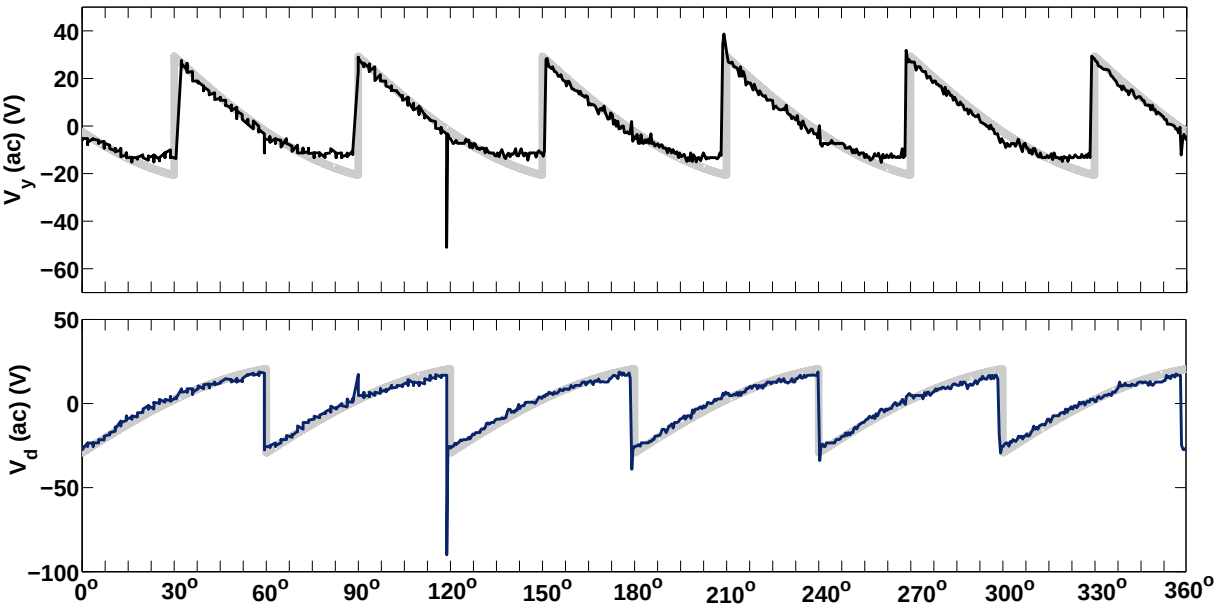


Figure 6.13: Measured ripple voltage V_{ripple} across DC blocking capacitor.

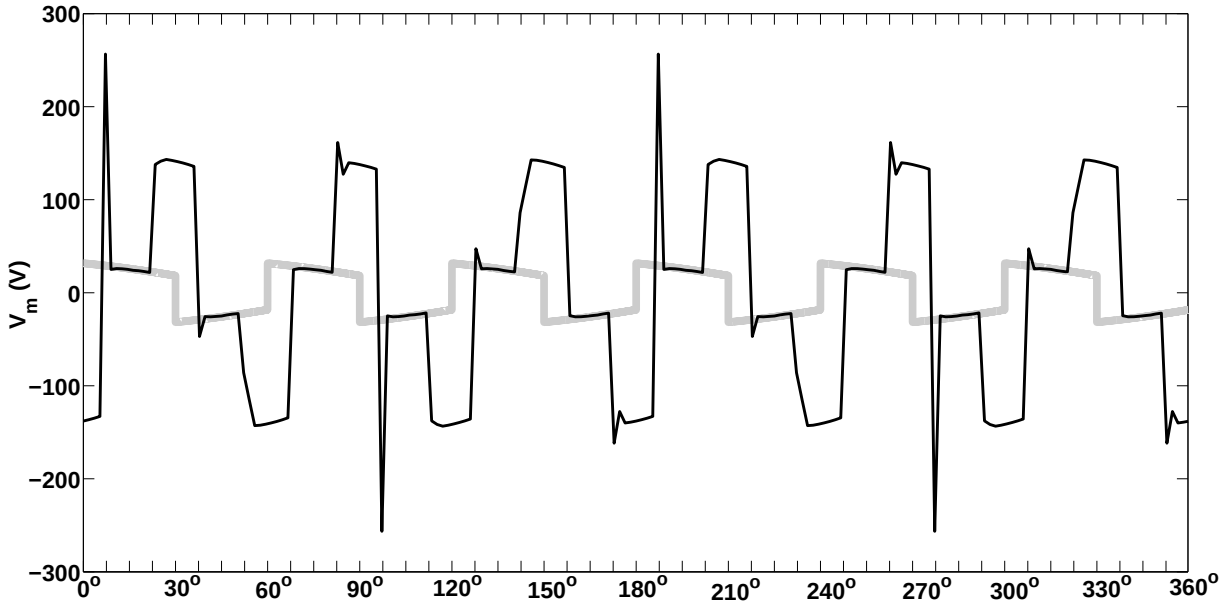


(a): Reinjection Transformer primary side **experimental** voltage $V_{y_{ac}}$ and $V_{d_{ac}}$.

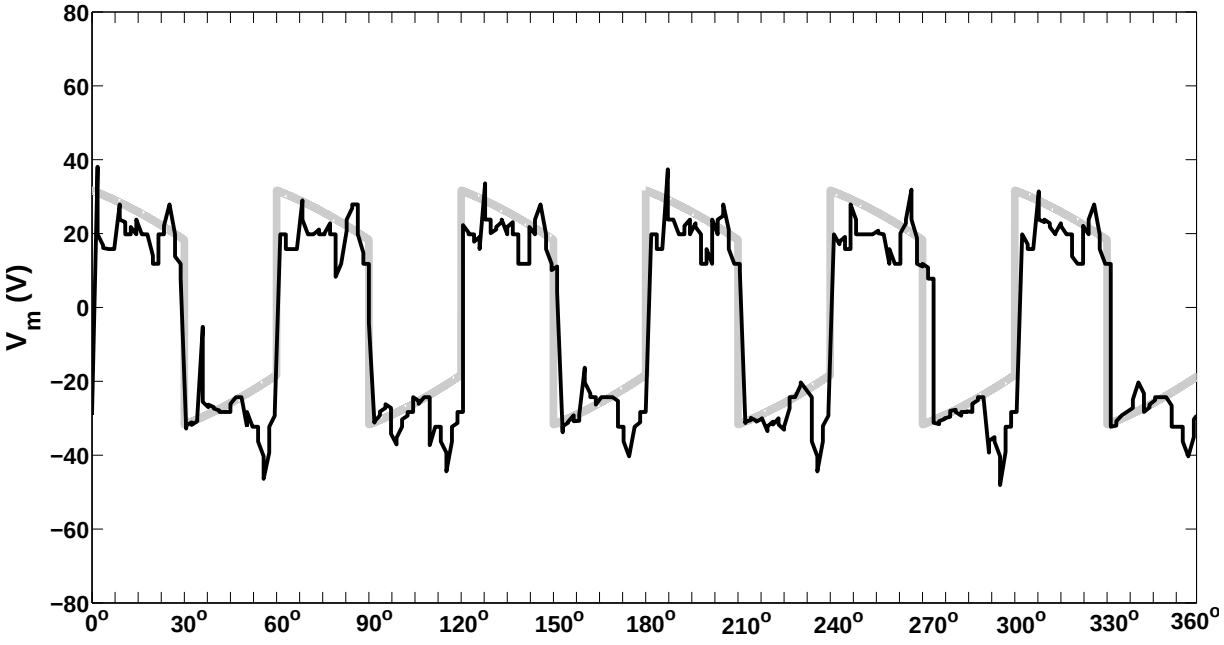


(b): Reinjection Transformer secondary side **experimental** voltage $V_{y_{ac}}$ and $V_{d_{ac}}$.

Figure 6.14: Reinjection Transformer secondary side voltage V_m with 'small' C_{sn}.

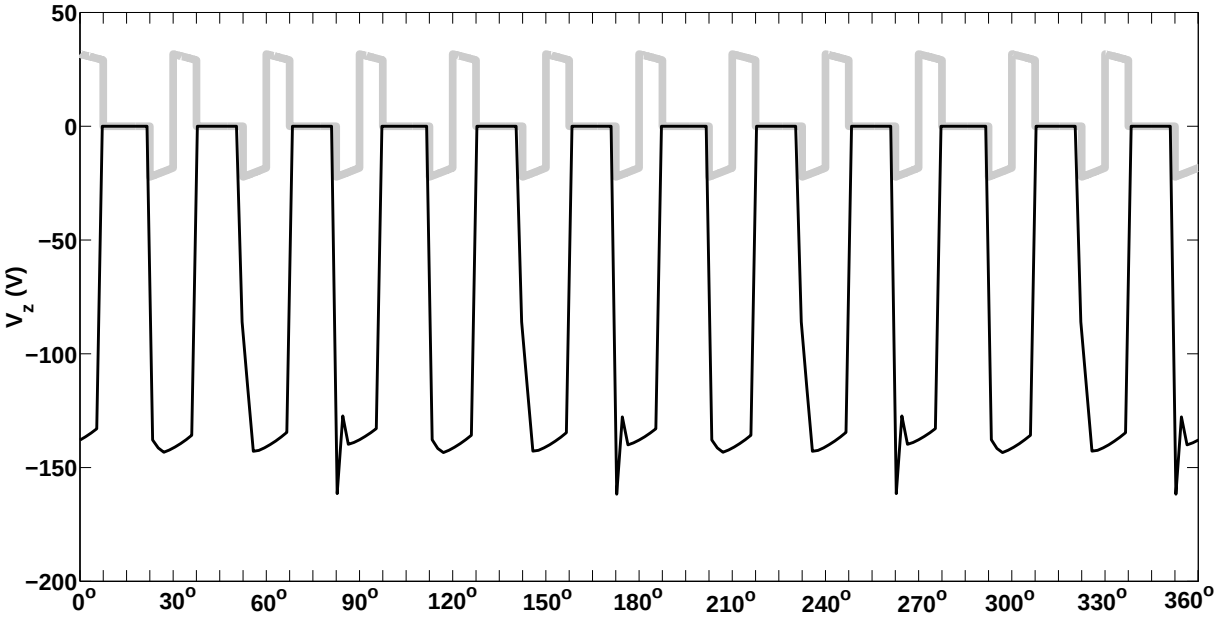


(a): Reinjection Transformer secondary side **PSCAD/EMTDC** voltage V_m.

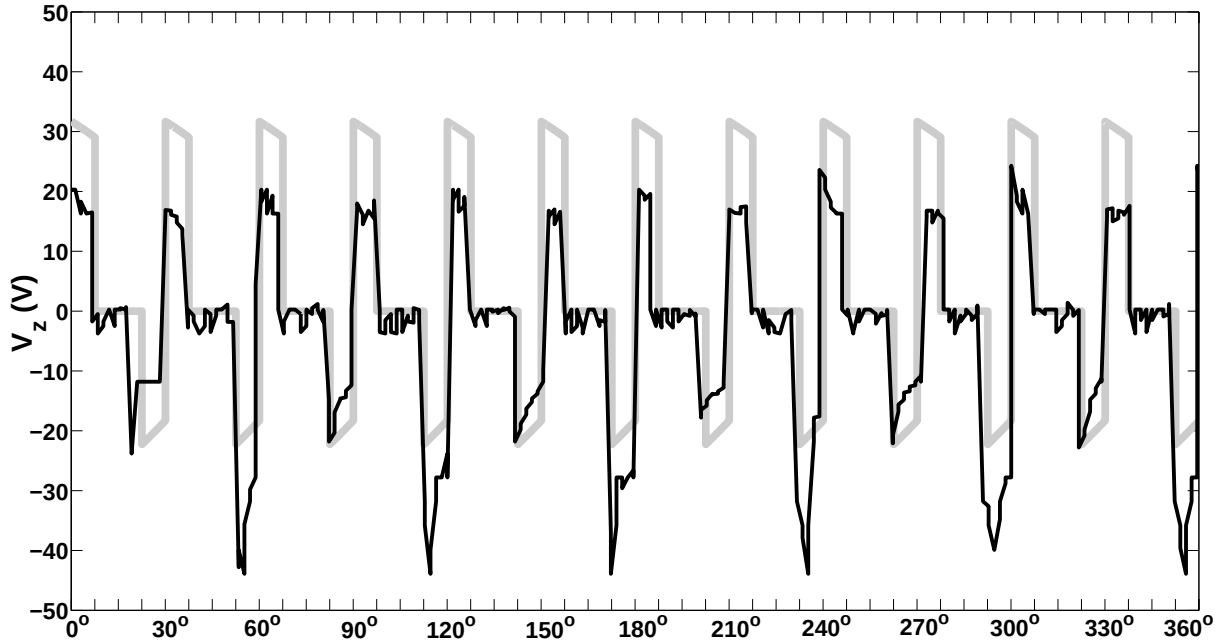


(b): Reinjection Transformer secondary side **experimental** voltage V_m, $C_{sn} = 0.01$ μF.

Figure 6.15: Reinjection Transformer secondary side voltage V_m with 'small' C_{sn}.

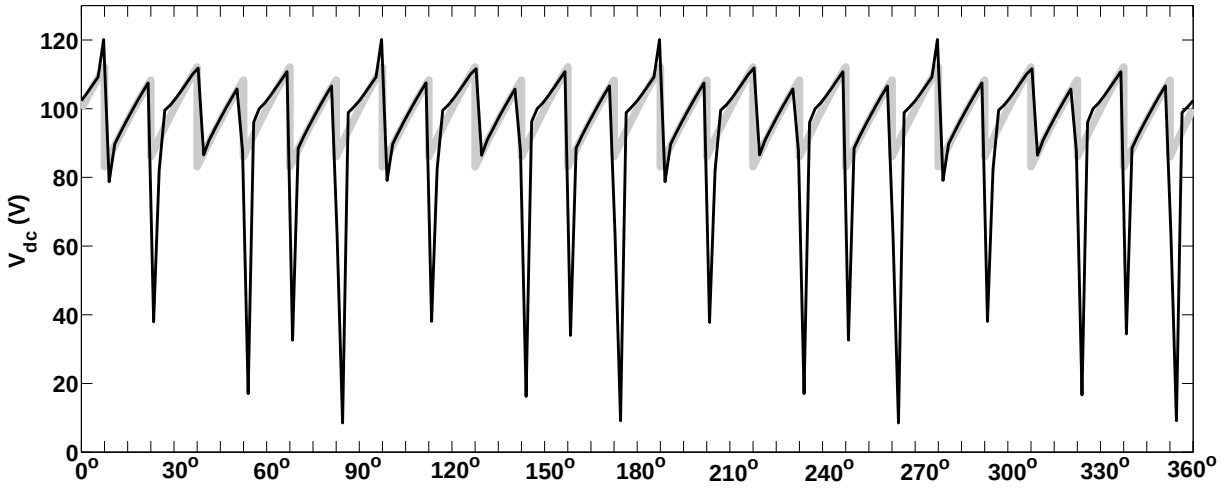


(a): Reinjection **PSCAD/EMTDC** voltage V_z.

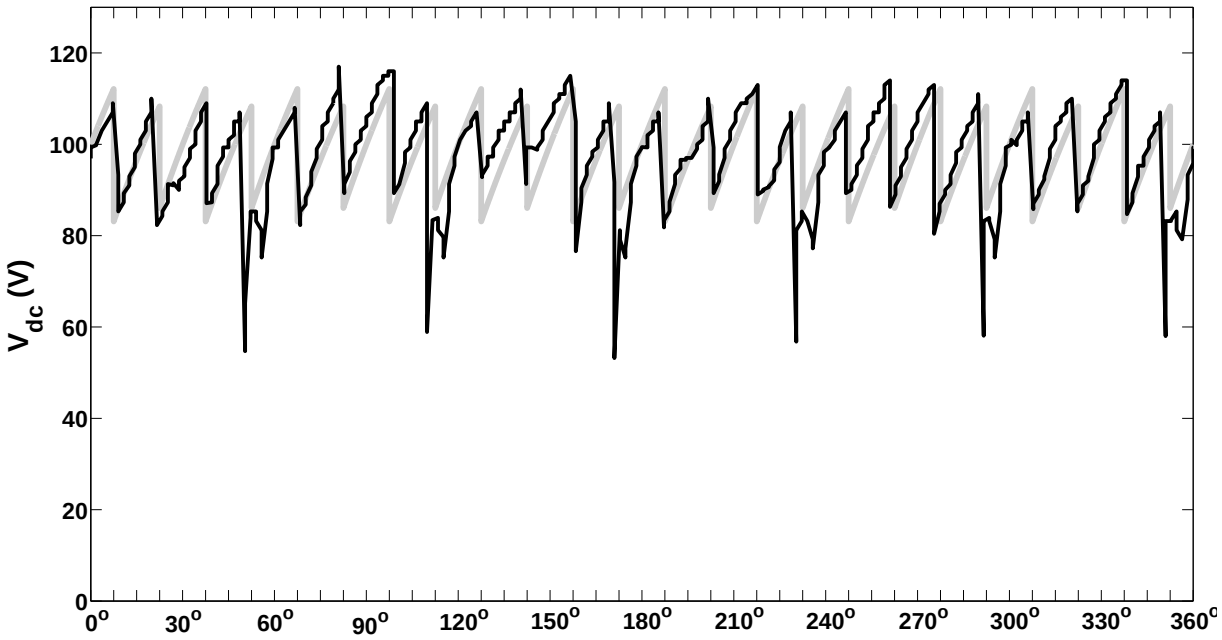


(b): Reinjection **experimental** voltage V_z, $C_{sn} = 0.01$ μF.

Figure 6.16: DC Reinjection voltage V_z with 'small' C_{sn}.

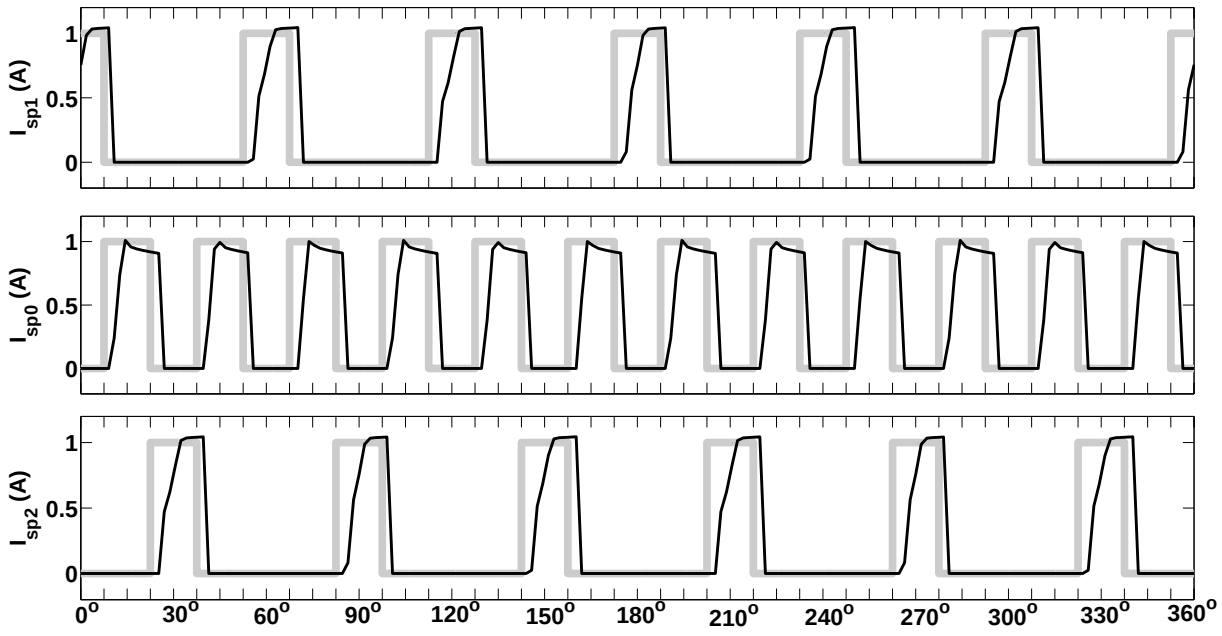


(a): DC **PSCAD/EMTDC** voltage V_{dc}.

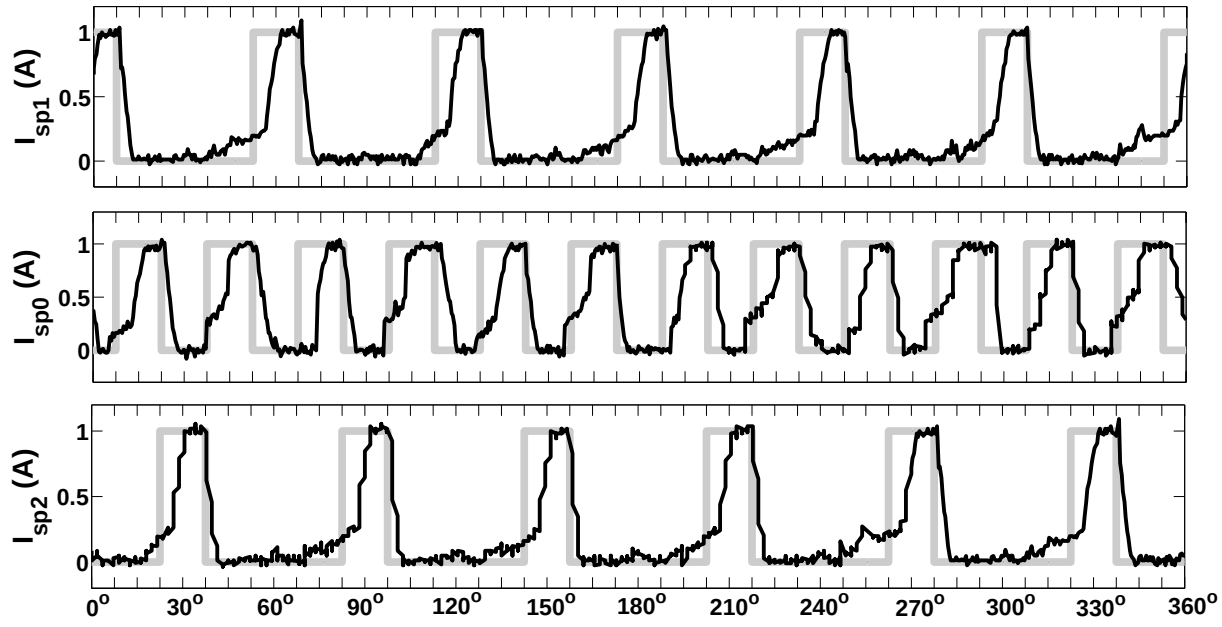


(b): DC **experimental** voltage V_{dc}, $C_{sn} = 0.01$ μF.

Figure 6.17: DC voltage waveform V_{dc} with 'small' C_{sn}.

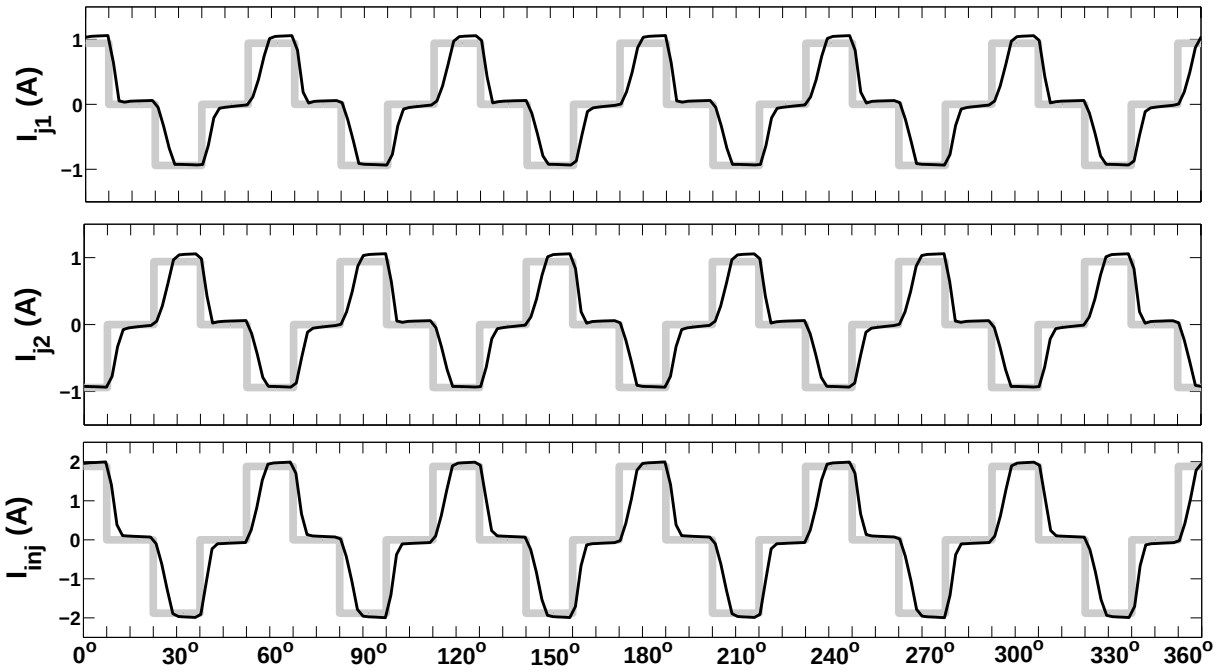


(a): I_{sp1}, I_{sp0} and I_{sp2} **PSCAD/EMTDC** waveforms.

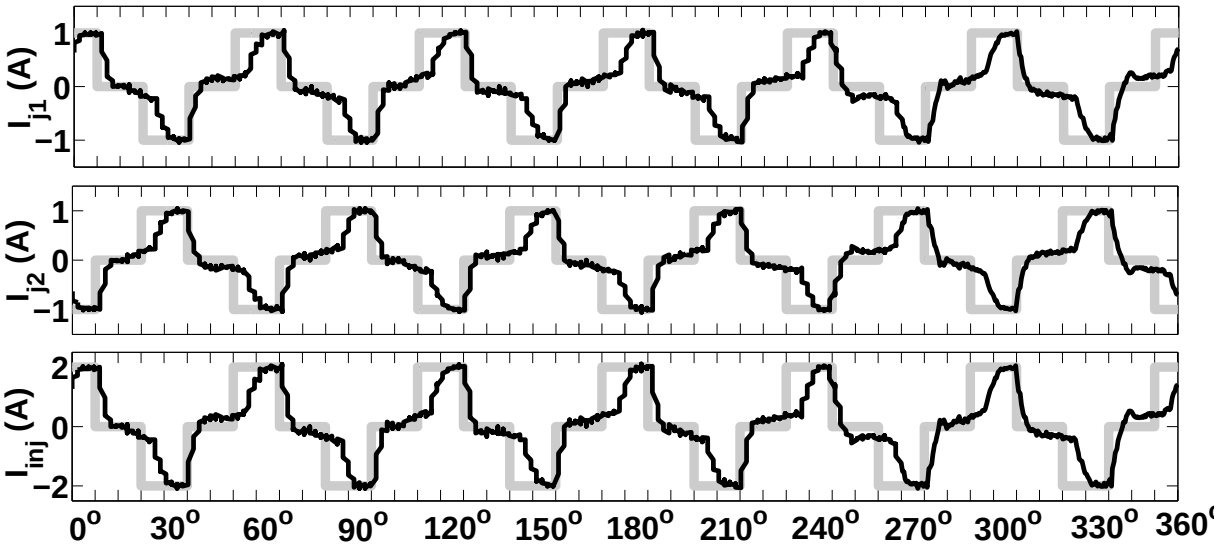


(b): I_{Sp1}, I_{Sp0} and I_{Sp2} **experimental** waveforms, $C_{sn} = 1$ μF.

Figure 6.18: Currents through reinjection IGBT with 'very large' C_{sn}.

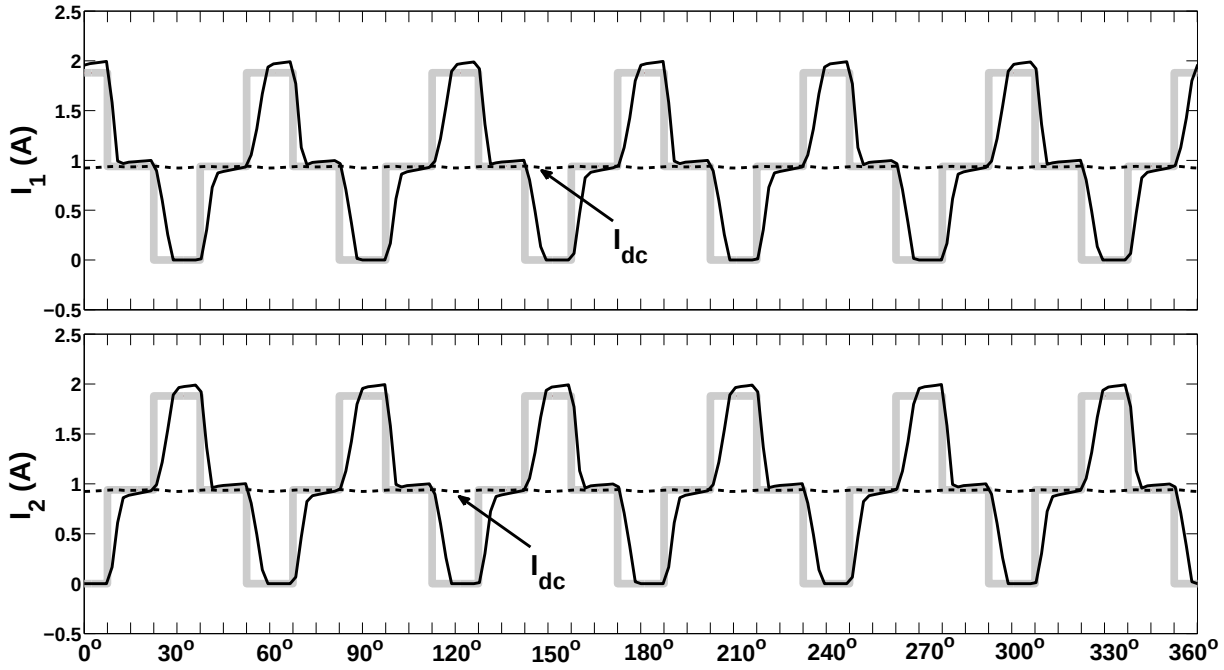


(a): I_{j1}, I_{j2} and I_{inj} **PSCAD/EMTDC** waveforms.

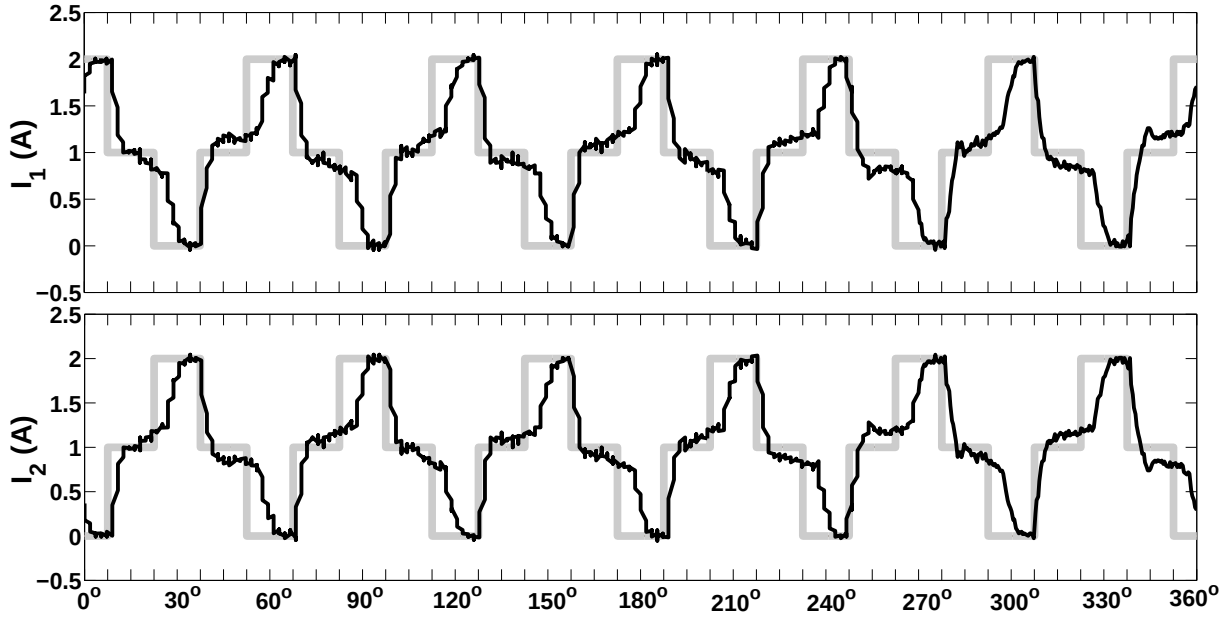


(b): I_{j1}, I_{j2} and I_{inj} **experimental** waveforms, $C_{sn} = 1$ μF.

Figure 6.19: Reinjection current waveforms with 'very large' C_{sn}.

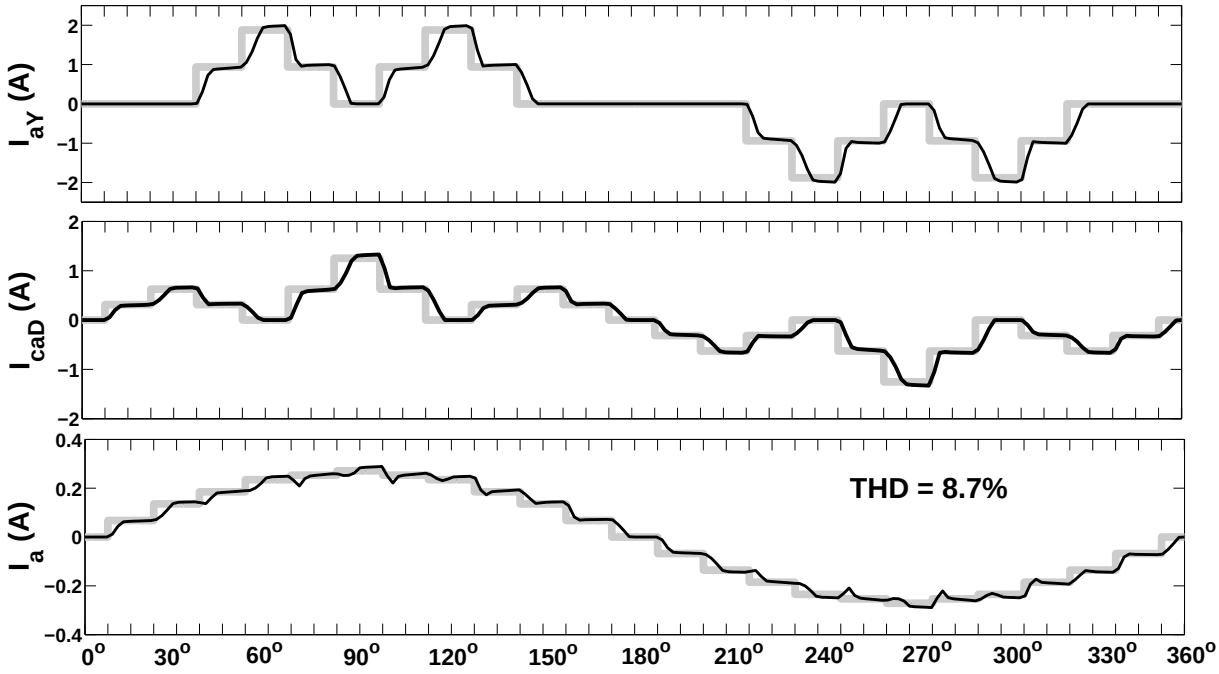


(a): I_1 and I_2 **PSCAD/EMTDC** waveforms.

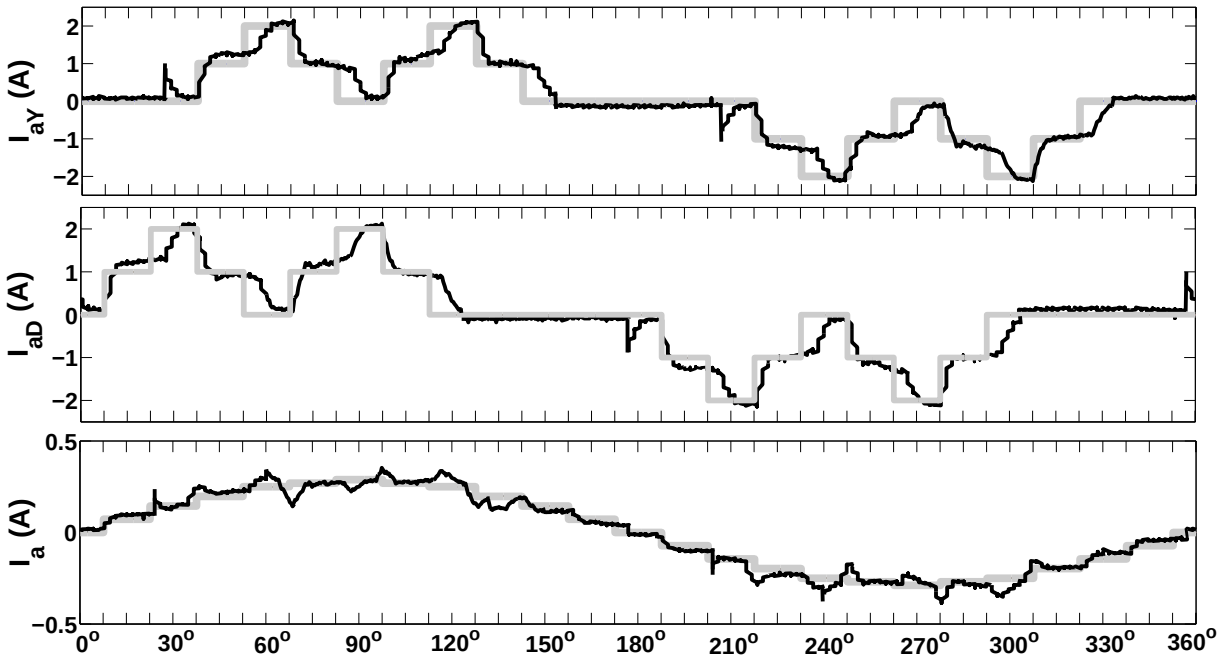


(b): I_1, I_2 **experimental** waveforms, $C_{sn} = 1$ μF.

Figure 6.20: DC bus current waveforms with 'very large' C_{sn}.

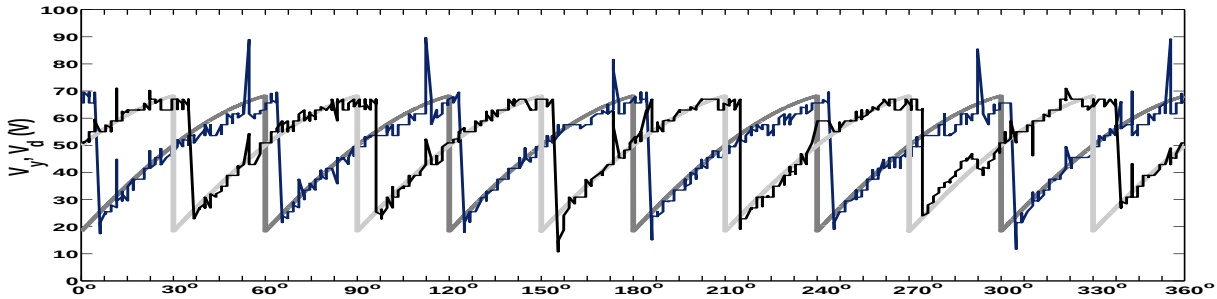


(a): I_{aY}, I_{caD} and I_a **PSCAD/EMTDC** waveforms.

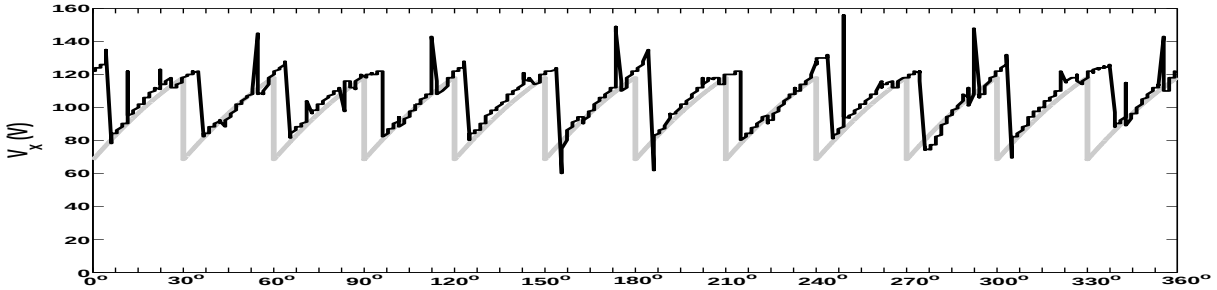


(b): I_{aY}, I_{aD} and I_a **experimental** waveforms, $C_{sn} = 1$ μF.

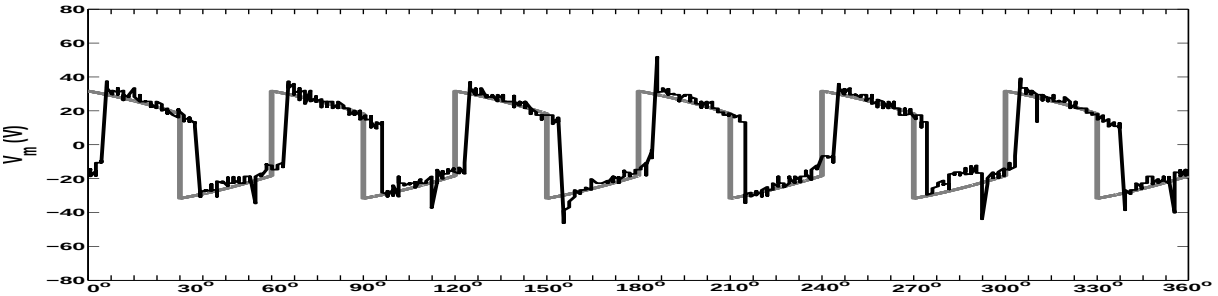
Figure 6.21: AC-side current waveforms with 'very large' C_{sn}.



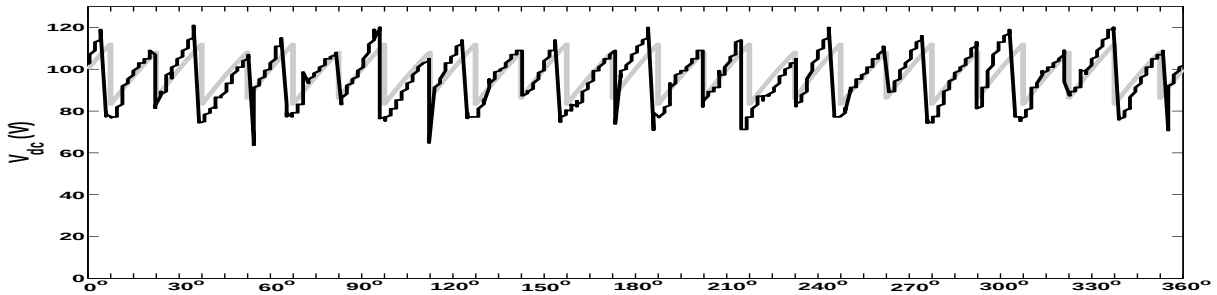
(a): DC voltage waveform V_y and V_d.



(b): 12-pulse DC voltage waveform V_x.



(c): Reinjection Transformer secondary side voltage V_m.



(d): 3-level MLCR CSC DC voltage waveform V_{dc}.

Figure 6.22: Experimental DC-side voltage waveforms with 'very large' $C_{sn} = 1$ μF.

Chapter 7

COMPARATIVE STUDY BETWEEN LC CSC, PWM-VSC AND MLCR CSC

7.1 INTRODUCTION

There are now a number of well established technologies which are capable of realizing HVDC systems. The classical LC CSC has been in operation for more than 50 years now. In recent years, the technology of PWM-VSC is emerging to be an alternative approach. With the possibility of achieving self-commutation using thyristor based MLCR CSC (as demonstrated in the previous chapter), this concept has the potential to compete with these two established technologies. All these three technologies are fully capable of realising an HVDC system, and the converter power circuit design trade-offs between these three alternatives are not apparent. This chapter presents an examination of these topologies from the point of view of power semiconductor requirements, reactive support requirements, converter losses, fault response, etc. The New Zealand HVDC converter is used to develop a comparative evaluation of the three alternative power converters for trade-off studies.

7.2 COMPARATIVE STUDY BETWEEN LC CSC, PWM VSC AND 7-LEVEL MLCR CSC

HVDC power converters are used in either sending or receiving mode; this evaluation will concentrate on sending power from an AC source (generator). The cost of a HVDC power converter depends on many factors, such as power capacity to be transmitted, type of transmission, location and environmental conditions, safety and other regulatory requirements, etc. Even when these are available, the options available for optimal design (different commutation techniques, variety of filters, transformers etc.) render it difficult to give an exact cost figure for a HVDC converter. With such wide range of variability, the definitive evaluation appears to be a cumbersome task; however, an attempt using the New Zealand Inter Island HVDC Pole 2 [Griffiths and M.Zavahir 2008] to develop a comparative evaluation of the three alternative power converters for trade-off studies, is made here. Recently, an upgrade, known as the New Zealand Inter Island

HVDC Pole 3 Project, was completed where the existing HVDC Pole 1 based on mercury arc valves were replaced by thyristors.

The comparison criteria used for the evaluation include voltage, current and power ratings of the main power circuit components (including transformers, semiconductor switches, etc), quality of current waveforms in terms of harmonics, and losses in power semiconductors. However, the trade-off of power converter using these approaches is a function of market trends, economic factors and engineering developments, and would vary with time and location; a preliminary estimate of these indices together provides a basis for making an initial trade-off assessment among these schemes. A comparison between PWM-VSC and LC CSC in terms of site aspects (overall footprint, building size etc) is provided by [Sellick and Akerberg 2012] where PWM-VSC is shown to use only 77% of the overall site area than that of LC CSC, largely due to no reactive power compensation requirements of PWM-VSC. This is an encouraging sign for MLCR CSC as it allows higher power thyristors to be used while having no reactive power compensation requirements.

The New Zealand HVDC Pole 2 (Table 7.1) is used as a benchmark model. The HVDC link now consists of one permanently operating pole: Pole 2 (commissioned in 1991) operating at 350 kV, which uses thyristor conversion technology. An older pole (Pole 1), which used mercury arc valve technology, was fully decommissioned in 2012. A replacement pole (Pole 3) was commissioned in 2013. The Pole 2 converter rating of 500 MW (base power) at 350 kV (base DC voltage) from a 220 kV (base AC voltage) AC input is used for numerical comparison of the design variables.

Table 7.1: p.u. Quantities for NZ HVDC Pole 2.

Transformer MVA(Pri), (VA_B)	652.6 MVA
Transformer MVA(Sec), (VA_B)	326.1 MVA
Base Frequency, (f_B)	50 Hz
AC Base Source voltage, (V_{Bs})	220 kV
Converter Base voltage, (V_{Bsec})	143.9 kV
DC Base voltage, (V_{Bdc})	350 kV
AC Base Source current, (I_{Bs})	1.71 kA
DC Base current, (I_{Bdc})	1.42 kA
AC Base Source Impedance, (Z_{Bac})	128 Ω
DC Base Source Impedance, (Z_{Bdc})	246 Ω
AC Base Inductance, (L_{Bac})	400 mH
DC Base Inductance, (L_{Bdc})	78 mH

Using the transformer primary and secondary MVA rating, turns ratio (k_n) for LC CSC and MLCR CSC = 1.53. Turns ratio of the transformer for PWM-VSC is discussed later on.

7.2.1 Choice of Semiconductor Switches

For reliable and efficient operation, the proper choice of the semiconductor switches is a must. The important factors in this choice include:

- Switch controllability;
- Switching frequency limitations;
- Blocking voltage and current rating;
- Maximum operating temperature permitted.

To realise a high blocking voltage, all the three power converters have semiconductor switches connected in series to share the blocking voltage. To keep the number of switches to a reasonable level, the highest possible voltage rated switch must be used. Moreover, snubber circuits are put in parallel across each device to ensure equal voltage sharing among the switches in LC CSC and PWM-VSC. However, as the MLCR CSC switches are turned on and off under zero current condition, snubber circuits can be avoided. Also, the number of switches in series needs to be minimised so that snubber circuits can also be minimised. In terms of switching frequency limitations, thyristors and IGCTs have maximum frequency limitations of around 500 Hz whereas IGBTs are operated $\leq$ 2 kHz in most of the PWM-VSCs worldwide. Since the reinjection switches of the MLCR CSC must have a controllable turn-off with uni-directional current, IGCTs without the anti-parallel diode are best option.

The viable choices for power semiconductors for each converter topology are summarized in Table 7.2.

Table 7.2: Semiconductor Switches for three different HVDC Converters.

	LC CSC	PWM-VSC	MLCR CSC
Switch	SCR	IGBT + Diode	SCR + IGCT

The choice of a particular semiconductor switch also depends on the average current through the switch. For LC CSC the average current carried by each thyristor leg equals to (1/3) I_{dc}. In case of PWM-VSC arm current flows in the IGBT and the diode unequally resulting in asymmetrical device currents, but equal to (1/3) I_{dc}. However, unlike the LC CSC and PWM-VSC power converters where the switch currents are entirely DC, the MLCR CSC has a varying (Reinjected AC current + I_{dc}) DC current due to current reinjection by the auxiliary reinjection bridge. To quantify these characteristics, the average current for each of the three power converters is listed in Table 7.3. To achieve appropriate blocking voltage, N number of semiconductor devices are connected in series. To keep the number of switches to a reasonable level, highest possible voltage rated switch is used; however, a prominent feature of this series connection is switch de-rating.

Table 7.3: Power Semiconductor Currents (RMS) and Voltages (p.u.).

CSC		7-level MLCR CSC				PWM-VSC	
I_{thy}	$0.577I_{dc}$	I_{thy}	$0.671I_{dc}$	I_{igct}	$0.4082I_{dc}$	I_{leg}	$0.45I_{dc}$
I_s	1.5768 I_{dc}/k_n	I_s	1.5971 I_{dc}/k_n	–	–	I_s	0.7407 I_{dc}/k_n
$\frac{V_{block}}{V_{dc}}$	$\frac{1}{N_{csc}+1}$	$\frac{V_{block}}{V_{dc}}$	$\frac{1}{N_{mlcr}+1}$	$\frac{V_{block}(igbt)}{V_{ll}}$	$\frac{0.732}{k_n}$	$\frac{V_{block}}{V_{dc}}$	$\frac{1}{N_{vsc}+1}$

Table 7.4: Semiconductor switches selection comparison for 500 MW, 350 kV 12-pulse converter (175 kV 6-pulse converter).

	LC CSC	PWM-VSC	MLCR CSC	
Part No	5STP 20N8500	5SNA 2000K451300	5STP 20N8500	5SHY 42L6500
Type	Thyristor	IGBT+Diode	Thyristor	IGCT
Blocking Voltage	8 kV	4.5 kV	8 kV	6.5 kV
Derated Blocking Voltage	4 kV	2.25 kV	4 kV	3.3 kV
Devices per leg	45	79	45	33
Total number of devices	270	474	270	231
Average on-state current	2 kA	2 kA	2 kA	3.8 kA

Switch de-rating is done in order to ensure that if failure of any one of the switches in series occurs, the rest of the switches are able to handle the increased blocking voltage. Typically, the semiconductor switches are de-rated to 50%-70% of the voltage blocking capability listed by the manufacturer. Usually, a N+1 "redundancy" is used. The blocking voltage is determined as:

$$V_{blocking} = \frac{V_{dc}}{N+1} \tag{7.1}$$

Table 7.4 shows (highest blocking voltage available from ABB) semiconductor switch selection for the different power converter parameters.

7.2.2 Choice of AC-side components

The most common AC-side components include: transformers and line filters.

Transformers

The rating of a transformer is governed by the peak voltage and the RMS current, respectively. The three-phase VA ratings are calculated as:

$$VA = \frac{3}{\sqrt{2}} V_{ln_{pk}} I_s \tag{7.2}$$

For LC CSC, the RMS value of I_s is given by:

$$I_s = \frac{1.5768}{k_n} I_{dc} \tag{7.3}$$

$$V_{ln_{pk}} = 0.33 k_n V_{dc} \tag{7.4}$$

For 7-level MLCR CSC, the RMS value of I_s is given by:

$$I_s = \frac{1.5970}{k_n} I_{dc} \tag{7.5}$$

$$V_{ln_{pk}} = 0.294 k_n V_{dc} \tag{7.6}$$

Using nominal V_{dc} = 350 kV, transmitted DC power of 500 MW, AC-side grid voltage of 220 kV, and assumed modulation index of m = 0.85, the secondary side AC voltage using V_{ll} = 0.612 × m ×V_{dc} = 182.21 kV. Turns ratio ($k_n : \sqrt{3}$) of PWM-VSC transformer is = 1.207:1.732. For this converter, the RMS value of I_s is given by:

$$I_s = \frac{0.7407}{k_n} I_{dc} \tag{7.7}$$

$$V_{ln_{pk}} = 0.666 k_n V_{dc} \tag{7.8}$$

The AC-side transformer MVA ratings (p.u) are summarized in Table 7.5. It can be seen that the MVA rating of the MLCR CSC transformer is reduced.

Table 7.5: Transformer rating (p.u.) for three different HVDC Converters.

Converter	MVA / P_{dc}
CSC	1.1
MLCR CSC	1.00
PWM-VSC	1.046

AC-side line currents and Filters

The phase voltage and line current on the AC-side of the 12-pulse LC CSC is shown in Figs. 7.1-7.2 which has characteristic harmonic currents of order $12n \pm 1$. The line current THD is equal to 10.82% without any line current filters. AC-side filters are required to meet power quality standards (IEEE 519 etc). Additionally, during the power conversion process the LC CSC consumes reactive power which is compensated by the filter and capacitor banks. A detailed evaluation of such an AC-DC filter design for the Three-Gorges Ghangzhou ± 500 kV HVDC project is presented by [Bergdahl and Das 2012]. The different filter solutions are needed due to different AC system conditions at the two ends of the converter. A typical rating for a

representative AC-side filter is 0.35 p.u. and the amount of reactive power compensation needed is calculated based on maintaining a power factor of 0.85.

The AC voltage output contains the fundamental AC component plus higher-order harmonics derived from the switching of the PWM-VSC, as shown in Figs. 7.3 - 7.4. PWM output waveform contains harmonics $\frac{f_s}{f_g} \pm n$ where f_s: switching frequency, f_g: fundamental grid frequency, n: odd integer. For a 2-level PWM-VSC, line current THD of 4.58% without any line current filters is obtained. Usually, with $f_s = 2$ kHZ, tuned AC filters to reduce harmonics beyond the 40th harmonic are required. Typical quality factor is between 0.5% and 5% and AC-filter rating is at 0.15 p.u. Phase reactors are used in PWM-VSC for controlling both the active and reactive power flow by regulating currents through them. The phase reactors are usually in the range of 0.1 p.u to 0.2 p.u.

The MLCR CSC produces high quality line current waveforms as seen from Figs. 7.5-7.6 with line current THD = 2.78%. It is clear that unlike the LC CSC and PWM-VSC, the MLCR CSC does not require any AC-side filter and reactive power compensator as even with thyristors, it can be switched on with a negative firing angle.

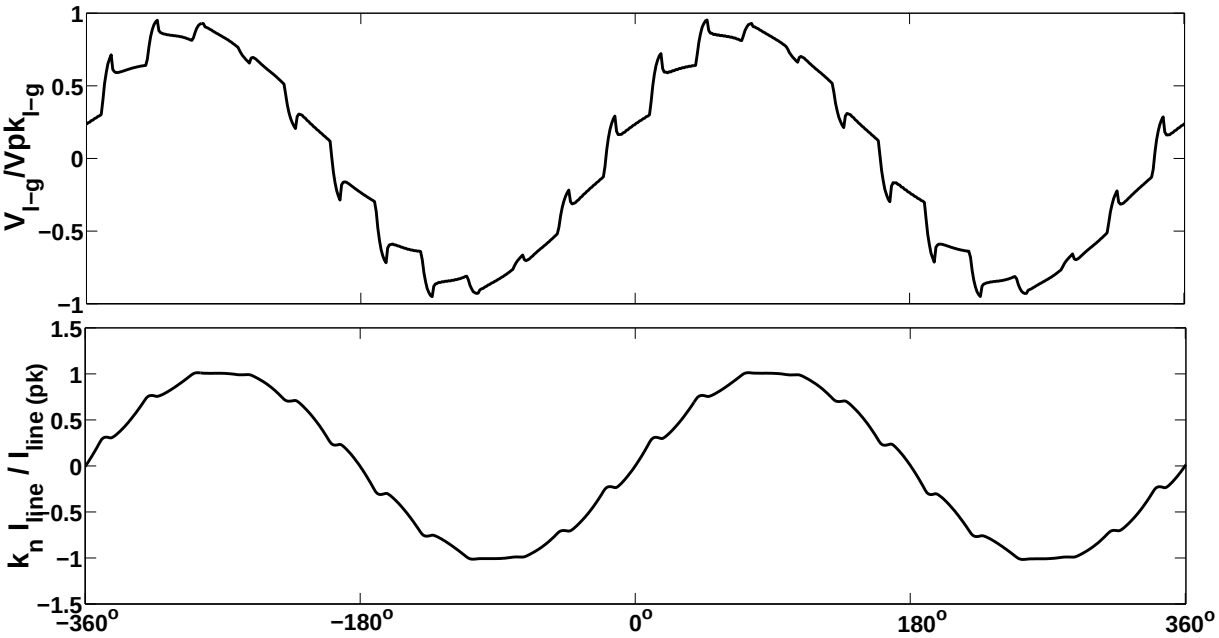


Figure 7.1: Voltage and current waveforms for LC CSC.

Table 7.6 shows the most dominant harmonic number for the three converters based on which AC-side filters are calculated.

Table 7.6: Lowest Harmonic Pulse Number for three different HVDC Converters.

	LC CSC	PWM-VSC	MLCR CSC
Dominant Harmonic number	12	40	72

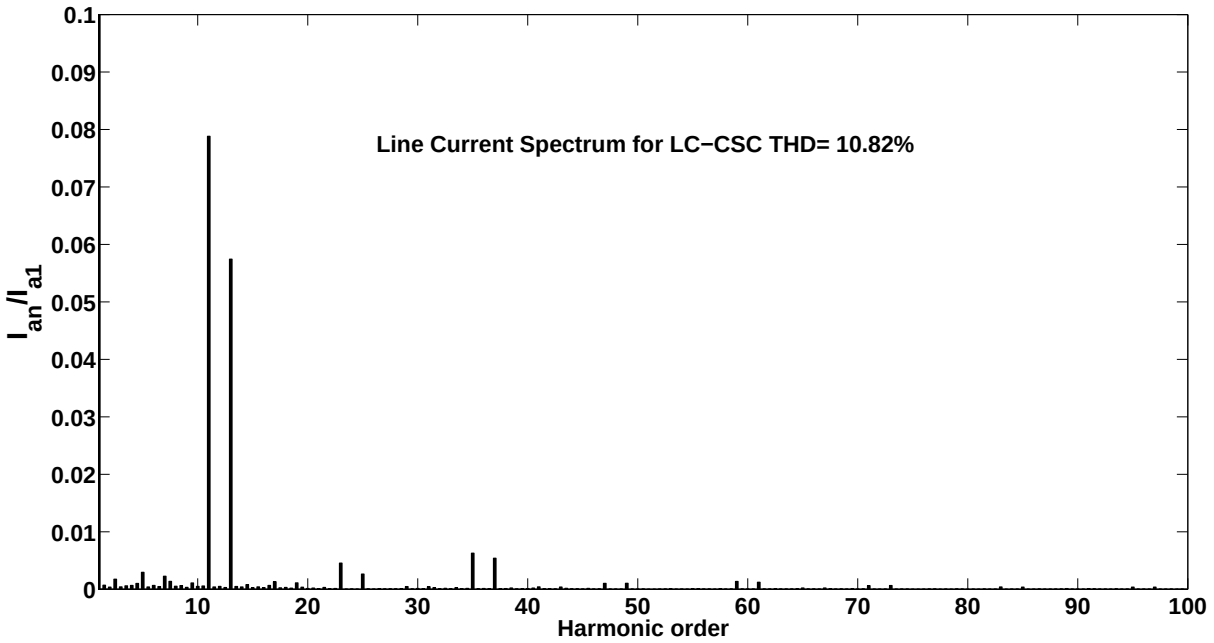


Figure 7.2: Line current THD for LC CSC.

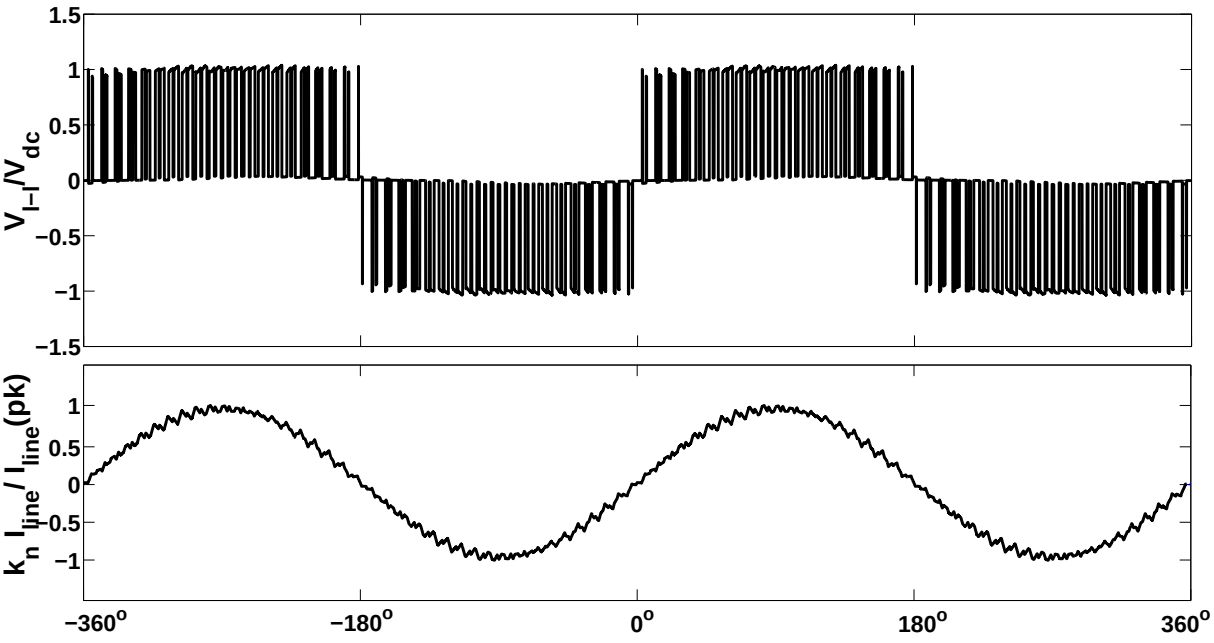


Figure 7.3: Voltage and current waveforms for PWM-VSC.

7.2.3 DC-side components

The smoothing reactor is usually designed to prevent commutation failures and to smooth the ripple in I_{dc} to prevent I_{dc} from becoming discontinuous at light loads. Considering the two design aspects into account, the size of smoothing reactors is often selected in the range of 100

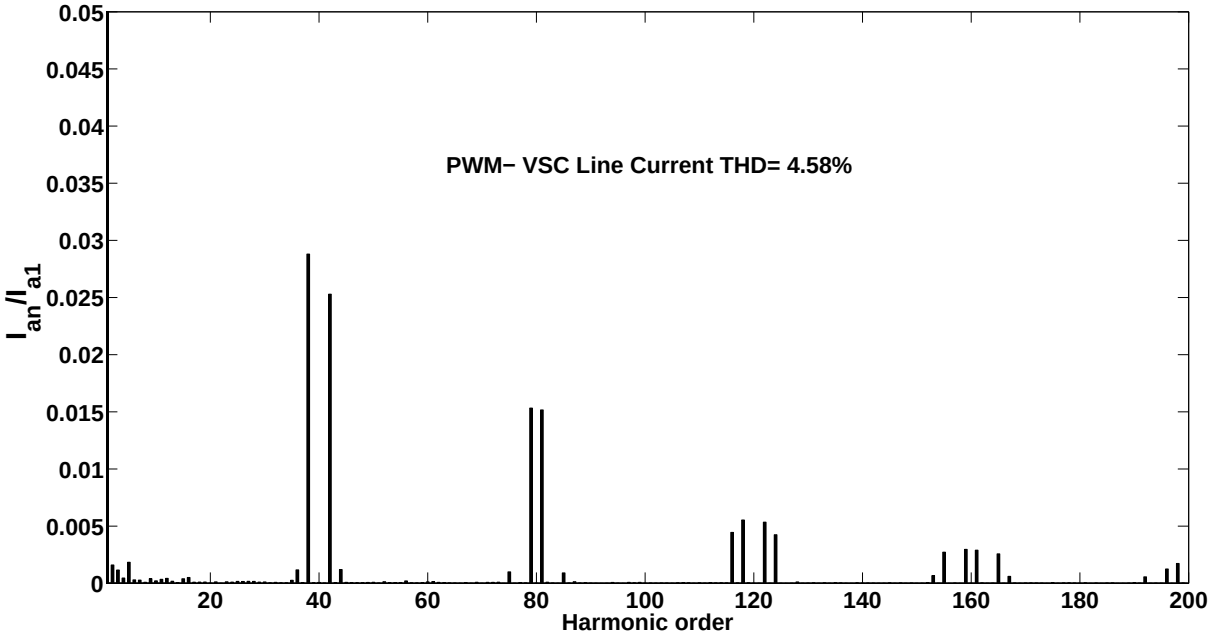


Figure 7.4: Line current THD for 2-level PWM-VSC.

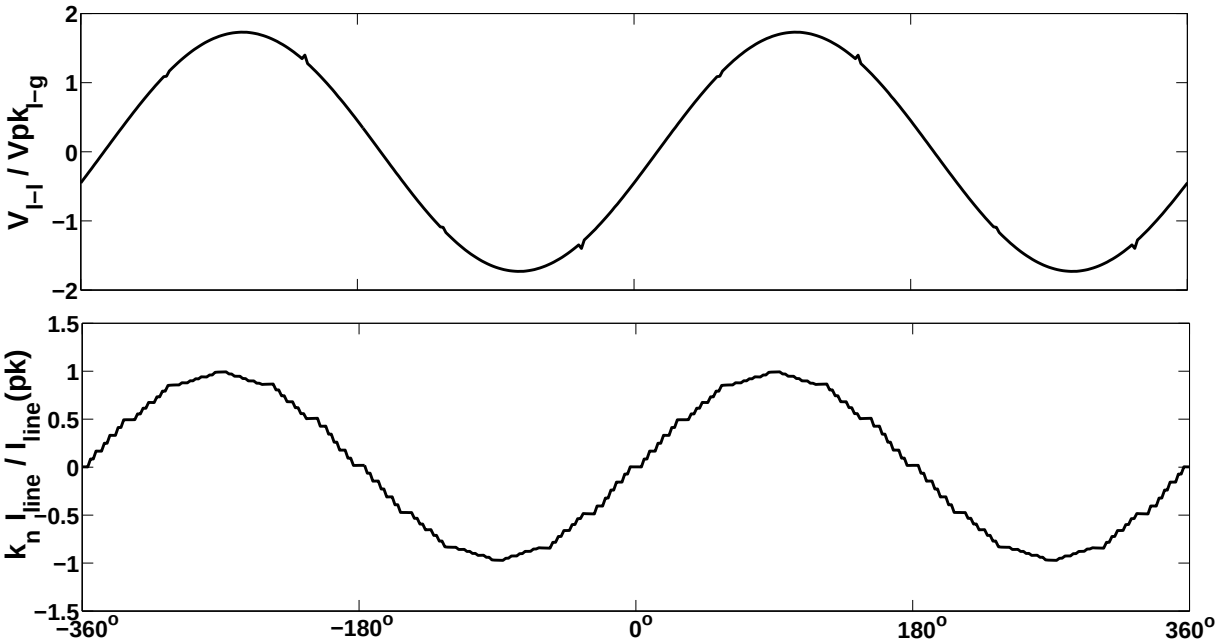


Figure 7.5: Voltage and current waveforms for MLCR CSC.

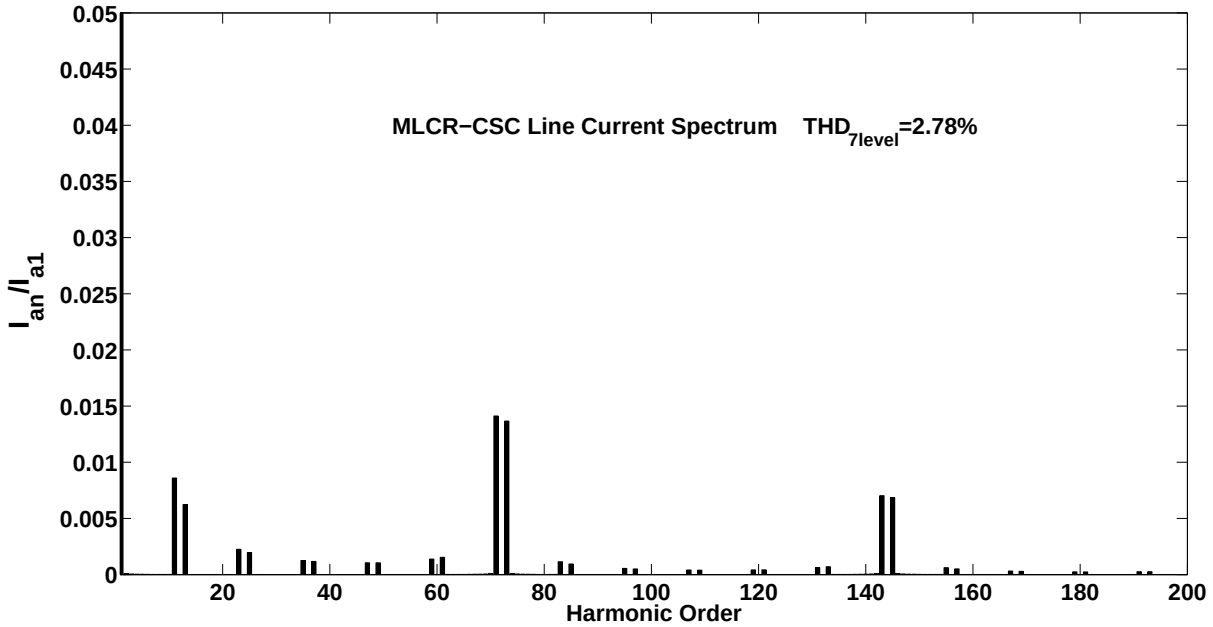


Figure 7.6: Line current THD for 7-level MLCR CSC.

to 300 mH for long distance DC links and 30 to 80 mH for back-to-back stations [Siemens 2011]. Using the calculated base inductance, smoothing reactors vary from 1.3 p.u. - 3 p.u. for long distance DC links to 0.3 p.u. - 1 p.u. for back-to-back links. The design evaluation of the DC reactor is not considered in detail in here, and can be found in [Kimbark 1971]. With the increase in pulse number for MLCR CSC from 12 to 72, the p.u. inductance varies from 0.2 - 0.5 p.u. for long distance DC links.

In PWM-VSC, the DC capacitor current contains harmonics, which results in ripple voltage on V_{dc}. Small ripple voltage requires a large capacitor, which has a slow response to voltage changes, whereas a small capacitor has faster dynamic response to changes in V_{dc}, allowing fast control of power at the expense of higher voltage ripple. A trade-off between voltage ripple and time constant of voltage is needed. Using the values in Table 7.1, DC base capacitance is 13 μF. The upper and lower limits of the size of DC-link capacitor is [Shire 2009]:

$$C_{dc} = \frac{P_{dc}}{2\omega V_{dc} \Delta V_d c} \tag{7.9}$$

$$C_{dc} = \frac{2\tau P_{dc}}{V_{dc}^2} \tag{7.10}$$

The upper and lower limits for this DC-link capacitor (assuming 10% ripple) are 65μF-8μF which gives a range of 5 p.u. - 0.6 p.u. where C_{dc} = 2 p.u. can be optimum choice.

7.2.4 Converter losses

LC CSC losses and efficiency calculation

The main kind of power semiconductor losses to be considered for LC CSC is the conduction loss, assuming other losses are negligible. Conduction losses result from the voltage drop across the device during the on-state condition. In LC CSC, thyristors operate at line frequency, and hence switching loss is considered negligible. The conduction loss P_{Lc} is calculated with the values of the equivalent straight line according to the following formula:

$$P_{Lc} = V_{T(TO)} \times I_{av} + r_T \times I_{av}^2 \times F^2 \tag{7.11}$$

Assuming that converter transformers, AC-side line filters and the smoothing inductor has a total efficiency of 99%, the loss summary for LC CSC is given in Table 7.7. The efficiency (η) of LC CSC = 98.8% using parameters from 5STP20N8500 data-sheet.

Table 7.7: LC CSC Loss Parameters.

Losses	Conduction Loss	Transformer loss	Total loss	Efficiency
LC CSC	0.0018 p.u.	0.01 p.u.	0.0118	98.8%

PWM-VSC losses and efficiency calculation

There are two main kinds of losses associated with PWM-VSC converter: Conduction loss and Switching loss. Other losses are assumed to be negligible. IGBT switching loss are characterized by discrete amounts of turn-on and turn-off energy per switching cycle while diode switching losses are defined by their reverse recovery energy. The switching loss is given by [Edrington *et al.* 2009]:

$$P_{Ls} = \frac{6}{\pi} f_s \cdot (E_{on,igbt} + E_{off,igbt} + E_{off,diode}) \frac{V_{dc}}{V_{ref}} \frac{i_L}{i_{ref}} \tag{7.12}$$

where f_s is the switching frequency, $E_{on,igbt}$ and $E_{off,igbt}$ are the turn-on and turn-off energies of the IGBT, $E_{off,diode}$ is the turn-off energy of the diodes, i_L is the peak value of the AC line current (assumed to be sinusoidal). The switching energies provided by data-sheets are given for a certain reference voltage V_{ref} and are equal to the blocking voltage of the IGBT, occurring before the corresponding commutation, and a reference current i_{ref} which is the on-state current after this commutation. The IGBT parameters are obtained from the 5SNA2000K451300 data-sheet to calculate switching loss.

In contrast to the switching losses, the conduction losses are directly dependent on the modulation function that is used. For sine-PWM, the conduction losses $P_{Lc}(igbt)$ and $P_{Lc}(diode)$ respectively are given as [Bierhoff and Fuchs 2004]:

$$P_{Lc}(igbt) = \frac{V_{ce} \cdot i_L}{2\pi} \cdot \big(1 + \frac{m\pi}{4}\cos(\phi)\big) + \frac{r_{ce} \cdot i_L^2}{2\pi}\big(\frac{\pi}{4} + \frac{2m}{3}\cos(\phi)\big) \tag{7.13}$$

$$P_{Lc}(diode) = \frac{V_{ce} \cdot i_L}{2\pi} \cdot \big(1 - \frac{m\pi}{4}\cos(\phi)\big) + \frac{r_{ce} \cdot i_L^2}{2\pi}\big(\frac{\pi}{4} - \frac{2m}{3}\cos(\phi)\big) \tag{7.14}$$

$$P_{Lc} = 6 \cdot (P_{Lc}(igbt) + P_{Lc}(diode)) \tag{7.15}$$

where m: modulation index, V_{ce}: IGBT threshold voltage, r_{ce}: IGBT slope resistance and ϕ: displacement angle.

The DC-link capacitor contributes power loss, but in the absence of the capacitor ESR data, this loss is neglected. The loss summary for PWM-VSC is given in Table 7.8. Efficiency (η) of PWM-VSC is 97.1%.

Table 7.8: PWM-VSC Loss Parameters.

Losses	Conduction Loss	Switching Loss	Transformer loss	Total loss	Efficiency
PWM-VSC	0.0058 p.u.	0.013 p.u.	0.01 p.u.	0.0288	97.1%

MLCR CSC losses and efficiency calculation

The main kind of power semiconductor losses to be considered for MLCR CSC are the main bridge losses and reinjection bridge losses. The main bridge losses are assumed to be the same as that of LC CSC. The conduction loss due to reinjection bridge is calculated using Eqn. 7.11 with F = 2.45. The switching loss is calculated with f_s = 300 Hz.

Table 7.9: MLCR CSC Loss Parameters.

Losses –>	Conduction Loss	Switching Loss	Transformer Loss	Total Loss	Efficiency
Main bridge	0.0018 p.u.	— p.u.	0.01 p.u.	—	—
Reinjection bridge	0.0015 p.u.	0.003 p.u.	0.01 p.u.	—	—
Total	0.0033 p.u.	0.003 p.u.	0.02 p.u.	.0263 p.u.	97.37%

With the results in Tables 7.7-7.9, it is clear that efficiency of the LC CSC is higher than both PWM-VSC and MLCR CSC. MLCR CSC has a marginally higher efficiency than the PWM-VSC, but both PWM-VSC and MLCR CSC will have considerably smaller site footprints largely due to very small or no reactive power compensation requirements. However, due to assumption

uncertainties in physical parameters and calculations, it would be more appropriate to consider the footprint design in detail.

A hyrbid thyristor-MLCR high current rectifier was proposed in [Murray 2008] for smelter applications. The total MLCR loss was calculated as 1.32% (1% transformer loss and 0.32% converter loss) excluding the switching loss. However, a much more realistic efficiency benchmark for all the converters should include switch dynamics, snubber losses, and control response etc.

7.2.5 Response to DC fault

LC CSC fault tolerance to DC line fault

Various studies on the performance of HVDC transmission line protection with different types of line fault have been elaborated in [Anderson 1999]. LC CSC is robust to DC line fault overcurrents because of their current-regulated nature and a large smoothing reactor on the DC side. Field results have shown that the short circuit current is of about 1 p.u. and an initial load current of 1 p.u gives a total current of about 2 p.u. Although this value is above the rated current, it is much smaller than the short-circuit current in an AC system [Kimbark 1971]. The over-voltage phenomenon caused by DC line fault has been described by [Kimbark 1970]-[Wrate *et al.* 1990] elaborately.

PWM-VSC fault tolerance to DC line fault

DC line faults (line-ground or line-line, less common because of line insulation and earth separation) on a PWM-VSC, result in the generation of large over-currents due to the discharge of the DC link capacitor which results in an increase in AC-side current. Also the IGBTs lose control and free-wheeling diodes conduct and feed the fault as the fault current is only limited by impedance of the transmission line. Because of the inherent topology of PWM-VSC, they are defenceless against DC faults and AC/DC protection must isolate the fault. The fault can either be cleared by the AC circuit breaker without protecting the PWM-VSC or by breakers at the DC-side [Candelaria and Park 2011].

DC circuit breakers are not an optimal choice currently, as no cost-effective alternative solution exists and it is very hard to develop a very fast mechanical circuit breaker [Franck 2011]. DC circuit breakers, used in traction applications, have been connected in series to meet the voltage requirements but series connection of the breakers imply that they are still prone to failure if the breakers do not commutate simultaneously [Flourentzou *et al.* 2009]. Solid state circuit breakers easily overcome the limitations of very fast switching times and voltage, but generate large

transfer losses - typically 30% of the losses of the PWM-VSC [Callavik *et al.* 2012]. [Callavik *et al.* 2012] presents details about the hybrid HVDC breaker.

Since DC line faults have a detrimental effect in the PWM-VSC operation and result in severe damage to the system component due to the resulting over-current, various studies are being carried out in this regard, more recent ones include [Yang *et al.* 2010] and [Yang *et al.* 2012].

MLCR CSC fault tolerance to DC line fault

A DC line fault is applied at the mid-point of the DC line when the MLCR CSC is operating with a real power order of 1000 MW, controlled by the sending station and a reactive power order of 2800 MVAR at the receiving station [Liu *et al.* 2007b]. The fault initially increases the DC current to try and maintain the specified power flow. However, during that process, the maximum I_{dc} is reached and the converter operates on constant-current control. Similarly the inverter end current reduces and is maintained at its minimum current setting. Upon detection of the fault, the sending-end converter changes to an inverter which clears the energy stored in the inductor, and after about 100 ms the normal operating conditions are re-established.

7.3 CONCLUSION

In this chapter the LC CSC, PWM-VSC and MLCR CSC have been evaluated for the New Zealand HVDC application with respect to switch requirements, reactive component requirements, line current harmonic obtained, operating losses, and response to DC line fault. A summary of the quantitative and qualitative characteristics of all three converters is presented in Table 7.10.

Table 7.10: Comparison summary for three different HVDC Converters.

	LC CSC	PWM-VSC	MLCR CSC
Efficiency (%)	98.8%	97.1%	97.37%
Transformer MVA rating	1.1 p.u	1.046 p.u	1 p.u
DC-side inductor rating	1.3 p.u. - 3 p.u	—	0.2 p.u. - 0.5 p.u.
DC-side capacitor rating	—	2 p.u.	–
Total power switches required	270 thyristors	474 IGBTs+ Diode	270 thyristors + 231 IGCTs
AC-side current THD (without filters)	10.82%	4.58%	2.78%
DC line fault tolerance	Good	Poor	Good

Chapter 8

GENERAL DISCUSSION AND FUTURE WORK

8.1 GENERAL DISCUSSION

Based on the multi-level current reinjection concept, 3-level MLCR CSC configuration has been studied in detail in this thesis and a prototype constructed for experimental validation. This converter combines current reinjection, soft switching and multi-level conversion, thereby permitting high efficiency, reliablity and low current distortion operation. The previous chapters include different converter configurations comparisons, firing strategies, steady state waveform analysis and experimental validation of the 3-level MLCR CSC. This section summarizes the general conclusions of this thesis.

- It is not possible to derive the ideal reinjection waveform required for perfect harmonic cancellation from a practical DC source. Two approximations were available: ESEDS and linear reinjection waveforms. The linear reinjection waveform, which has zero current duration during main bridge commutation instants was used to achieve self-commutation capability for a thyristor based main bridge.

- The method used to generate the multi-level reinjection waveforms supplied to the individual 6-pulse bridges is by addition and subtraction of the AC component of the DC bus current to and from the DC bus DC component. This is approximated by the steps created by a reinjection transformer.

- Theoretical waveforms and PSCAD/EMTDC simulations have shown that m-level MLCR-CSC produces high quality AC-side line current and DC-side voltage waveforms with very low content of 12-pulse related harmonics. Switching the main bridge at 50 Hz results low switching losses. The interesting fact with the zero current switching in MLCR CSC is the ability of the main bridge valves to commutate without the assistance of the line commutating voltage. However, questions about the ability to force the thyristors to turn-off are now addressed, based on the experimental results.

- The investigation of the performance under steady-state conditions showed a good agreement between the experimental and the theoretical AC-side line current waveforms. The reinjection current forces the main bridge thyristor to commutate under zero current, thereby allowing it to be switched at negative firing angles. From experimental results, it is observed that the deviation of the actual waveforms from the theoretical waveforms is mainly due the RC snubber across the reinjection IGBTs.

- With the experimental validation of the ability to turn-off the main bridge thyristors, a basic comparative study between LC CSC, PWM-VSC and MLCR CSC showed that the efficiency of MLCR CSC is slightly higher than that of PWM-VSC and it will have a much smaller foot-print than LC CSC. This opens up the possibility of a higher-level thyristor based MLCR CSC HVDC transmission system.

8.2 FURTHER WORK

The following investigations need to be carried out for MLCR CSC to exploit the advantages associated with it:

8.2.1 Laboratory Prototype of Parallel Connected MLCR CSC

To avoid the use of the reinjection transformer and reduce the number of reinjection switches by half, a prototype of parallel connected MLCR CSC can be built in the laboratory. The validation of properly distributing DC current using the multi-tapped reactor and still achieving self-commutation for thyristor based MLCR CSC can be presented.

8.2.2 Laboratory Prototype of MLCR CSC based STATCOM

A prototype STATCOM based on 3-level MLCR CSC can be developed in the laboratory. PSCAD/EMTDC has been used to show the fast dynamic response of the MLCR-CSC following disturbances, which makes the MLCR CSC an attractive alternative for STATCOM application [Liu *et al.* 2006]. The prototype could be built to test the validity and dynamic response of MLCR CSC based STATCOM.

8.2.3 Laboratory Prototype of ESEDS Reinjection MLCR CSC

A prototype MLCR CSC with self-commutated main bridge switches based on ESEDS reinjection can be developed in the laboratory. The harmonic distortion caused by ESEDS reinjection is

lower than linear reinjection, this fact can be validated by this prototype. A detailed comparison between self-commutated and thyristor based MLCR CSC can be carried out.

8.2.4 Extension into 7-level MLCR CSC with digital control

A comprehensive analysis of the thyristor based 7-level MLCR CSC has been presented in Appendix B-[4]. The 7-level MLCR CSC increases the pulse number from 12 to 72, thereby producing high quality AC-side current and DC-side voltage waveforms. The ability to switch thyristors with negative firing angle using 7-level reinjection bridge enables the converter to have a leading power-factor. A wide range of PSCAD/EMTDC simulation results are presented to evaluate performance of this converter including closed loop real power control. A hardware prototype for the 7-level MLCR CSC will confirm the very low distortion caused by this converter. However, the main limitation for 7-level high power MLCR CSC will be the unavailability of high power thyristors with fast reverse recovery time. IGCTs can be used for proof of concept.

8.2.5 Effect of RC snubber and ripple voltage on DC blocking capacitor for 7-level MLCR CSC

The effect of using different RC snubber combinations should be studied in detail to understand the effect on the AC-side current and DC-side voltage waveforms for a 7-level MLCR CSC. Similarly, the effect of voltage ripple on the DC-side voltage due to the DC blocking capacitor needs to be evaluated in depth.

8.2.6 7-level MLCR CSC with independent reactive power control

A prototype 7-level MLCR CSC BTB DC link with closed loop control can be an interesting topic for hardware development, one converter acting as the rectifier while the other as an inverter. Due to the fundamental switching of the main bridge switches in the MLCR CSC, this DC link will suffer from the inability to control reactive power at each end independently. The implementation of “multi-group” firing control [Murray 2008] will be a very challenging task for future research in this subject.

Appendix A

LINEAR WAVEFORM STEPPED APPROXIMATION

The stepped approximation for the m-level MLCR CSC DC bus current waveforms $I_1(\omega t)$ and $I_2(\omega t)$ using linear reinjection (as described in Section 3.4) can be approximated with the following time domain components in a complete cycle.

$$\frac{I_1(\omega t)}{I_L} = \begin{cases} (m-i-1) \\ i \\ (m-i-1) \\ i \\ (m-i-1) \\ i \\ (m-i-1) \\ i \\ (m-i-1) \\ i \\ (m-i-1) \\ i \end{cases}, \frac{I_2(\omega t)}{I_L} = \begin{cases} i, & \beta_i < \omega t < \beta_{i+1} \\ (m-i-1), & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ i, & \frac{2\pi}{6} + \beta_i < \omega t < \frac{2\pi}{6} + \beta_{i+1} \\ (m-i-1), & \frac{3\pi}{6} + \beta_i < \omega t < \frac{3\pi}{6} + \beta_{i+1} \\ i, & \frac{4\pi}{6} + \beta_i < \omega t < \frac{4\pi}{6} + \beta_{i+1} \\ (m-i-1), & \frac{5\pi}{6} + \beta_i < \omega t < \frac{5\pi}{6} + \beta_{i+1} \\ i, & \frac{6\pi}{6} + \beta_i < \omega t < \frac{6\pi}{6} + \beta_{i+1} \\ (m-i-1), & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ i, & \frac{8\pi}{6} + \beta_i < \omega t < \frac{8\pi}{6} + \beta_{i+1} \\ (m-i-1), & \frac{9\pi}{6} + \beta_i < \omega t < \frac{9\pi}{6} + \beta_{i+1} \\ i, & \frac{10\pi}{6} + \beta_i < \omega t < \frac{10\pi}{6} + \beta_{i+1} \\ (m-i-1), & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{A.1}$$

where $I_L = \frac{I_{dc}}{(m-1)}$ and $\beta_i = \frac{(2i-1)\pi}{12(m-1)}$, $\quad i = 1, 2, ..., m$.

The resulting phase 'A' current of the Y-Y connected bridge is:

$$\frac{I_{aY}(\omega t)}{I_L} = \begin{cases} 0, & 0 < \omega t < \frac{\pi}{6} + \frac{\pi}{12(m-1)} \\ i, & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ (m-i-1), & \frac{2\pi}{6} + \beta_i < \omega t < \frac{2\pi}{6} + \beta_{i+1} \\ i, & \frac{3\pi}{6} + \beta_i < \omega t < \frac{3\pi}{6} + \beta_{i+1} \\ (m-i-1), & \frac{4\pi}{6} + \beta_i < \omega t < \frac{4\pi}{6} + \beta_{i+1} \\ 0, & \frac{5\pi}{6} + \frac{\pi}{12(m-1)} < \omega t < \frac{7\pi}{6} + \frac{\pi}{12(m-1)} \\ -i, & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ -(m-i-1), & \frac{8\pi}{6} + \beta_i < \omega t < \frac{8\pi}{6} + \beta_{i+1} \\ -i, & \frac{9\pi}{6} + \beta_i < \omega t < \frac{9\pi}{6} + \beta_{i+1} \\ -(m-i-1), & \frac{10\pi}{6} + \beta_i < \omega t < \frac{10\pi}{6} + \beta_{i+1} \\ 0, & \frac{11\pi}{6} + \frac{\pi}{12(m-1)} < \omega t < 2\pi \end{cases} \tag{A.2}$$

The resulting phase 'A' current of the Y-D connected bridge is:

$$\frac{I_{caD}(\omega t)}{I_L} = \begin{cases} i/3, & \beta_i < \omega t < \beta_{i+1} \\ (m-i-1)/3, & \frac{\pi}{6} + \beta_i < \omega t < \frac{\pi}{6} + \beta_{i+1} \\ 2i/3, & \frac{2\pi}{6} + \beta_i < \omega t < \frac{2\pi}{6} + \beta_{i+1} \\ 2(m-i-1)/3, & \frac{3\pi}{6} + \beta_i < \omega t < \frac{3\pi}{6} + \beta_{i+1} \\ i/3, & \frac{4\pi}{6} + \beta_i < \omega t < \frac{4\pi}{6} + \beta_{i+1} \\ (m-i-1)/3, & \frac{5\pi}{6} + \beta_i < \omega t < \frac{5\pi}{6} + \beta_{i+1} \\ -i/3, & \pi + \beta_i < \omega t < \pi + \beta_{i+1} \\ -(m-i-1)/3, & \frac{7\pi}{6} + \beta_i < \omega t < \frac{7\pi}{6} + \beta_{i+1} \\ -2i/3, & \frac{8\pi}{6} + \beta_i < \omega t < \frac{8\pi}{6} + \beta_{i+1} \\ -2(m-i-1)/3, & \frac{9\pi}{6} + \beta_i < \omega t < \frac{9\pi}{6} + \beta_{i+1} \\ -i/3, & \frac{10\pi}{6} + \beta_i < \omega t < \frac{10\pi}{6} + \beta_{i+1} \\ -(m-i-1)/3, & \frac{11\pi}{6} + \beta_i < \omega t < \frac{11\pi}{6} + \beta_{i+1} \end{cases} \tag{A.3}$$

Appendix B

PUBLICATIONS

The following is a list of papers published/under review during the course of work on this thesis

1. B. P. Das, N. R. Watson, Y. H. Liu; *"Comparative Evaluation between LC CSC, PWM-VSC and MLCR CSC for Interconnection with the Electric Grid"*, in The 9^{th} IEEE conference on Industrial Electronics and Applications (ICIEA 2014), **Under review**.

2. B. P. Das, N. R. Watson, Y. H. Liu; *"Firing thyristors with negative firing angle using Multilevel Current Reinjection Concept: An experimental evaluation"*, in IEEE Transactions on Power Electronics, **Under review**.

3. B. P. Das, N. R. Watson, Y. H. Liu; *"Experimental Evaluation on the influence of RCD Snubber in a 3-level Thyristor based MLCR CSC"*, in Electric Power Components and Systems, **Accepted for publication**.

4. B. P. Das, N. R. Watson, Y. H. Liu; *"An Investigation into Thyristor based 7-level MLCR Current Source Converter"*, in Electric Power Components and Systems, Volume 42, Issue 2, Jan. 2014. DOI: 10.1080/15325008.2013.848498.

5. B. P. Das, N. R. Watson, Y. H. Liu; *"Application of the MLCR Concept to 6-pulse CSC"*, in IET Power Electronics, **Provisionally accepted for publication**.

6. M. S. Hwang, B. P. Das, A. R. Wood, N. R. Watson, Y. H. Liu; *"Capturing the Transient Evolution of Graetz Bridge Converter via the Harmonic State-Space"*, in International Transactions on Electrical Energy Systems (Formerly European Transactions on Electrical Power), Aug. 2013. DOI: 10.1002/etep.1787.
(Early View available)

7. B. P. Das, N. R. Watson, Y. H. Liu; *"m-level thyristor based MLCR CSC: A comparative study"*, in 2012 IEEE International Conference on Power System Technology (PowerCon '12), Oct.30-Nov.2 2012. DOI: 10.1109/PowerCon.2012.6401300.

8. B. P. Das, N. R. Watson, Y. H. Liu; *"Influence of zero width period on the AC-side line current harmonics of 5-level MLCR CSC"*, in 2012 IEEE International Conference on Power System Technology (PowerCon '12), Oct.30-Nov.2 2012. DOI: 10.1109/PowerCon.2012.6401306.

9. B. P. Das, N. R. Watson, Y. H. Liu; *"Comparative Evaluation of m-level Thyristor based MLCR CSC"*, in International Journal of Emerging Electric Power Systems, Volume 13, Issue 4, Oct. 2012. DOI: 10.1515/1553-779X.2978.

10. B. P. Das, N. R. Watson, Y. H. Liu; *"DC Ripple Reinjection: A Review"*, in International Journal of Emerging Electric Power Systems, Volume 12, Issue 5, Oct. 2011. DOI: 10.2202/1553-779X.2810.

11. B. P. Das, N. R. Watson, Y. H. Liu; *"Comparative Simulation Study between Gate Firing Units for HVDC Rectifier Based on CIGRE Benchmark Model"*, in Energy and Power Engineering, Volume 3, Issue 2, May. 2011. DOI:10.4236/epe.2011.32016.

Appendix C

PROBABLE CAUSES FOR DISTORTION - VOLTAGE SPIKES

Two possible causes of deviation from ideal MLCR output characteristics can be identified:

- Snubber Circuit Design
- Implementation of dead time in the reinjection circuit.

C.1 SNUBBER CIRCUIT DESIGN

When a power electronic converter stresses a power semiconductor device beyond its ratings, there are two ways of relieving the problem.

- Replace device by one whose ratings exceed the stresses.
- A snubber circuit can be added to the basic device to reduce the stresses to safe levels.

A trial and error method which used the basic assumption that IGBT current change linearly in time with a constant $\frac{di}{dt}$, was used to determine the snubber component values. However, actually $\frac{di}{dt}$ which may be different at turn-on and turn-off, is affected by the addition of the snubber circuit. This assumption provides the basis for a simple design procedure for a laboratory prototype. The final design will be somewhat different depending on what is revealed by laboratory measurements on the actual prototype circuit.

The final choice will be a trade-off between cost and availability of the semiconductor device with the required electrical ratings compared to the cost and the additional complexity of using a snubber circuit. The presence of stray inductances results in an over-voltage. For MLCR CSC applications, this over-voltage will be a function of the leakage inductances of the reinjection transformer. Hence, a reinjection transformer with low leakage inductance is critical in determining the reinjection switch rating. An approximate way to determine the leakage reactance

is to apply a short-circuit across the secondary. Thus from the Short Circuit test of the reinjection transformer, the leakage reactance is calculated to be 1.242 Ω for a transformer with base impedance of 160 Ω ((400V)^2/1kVA). Therefore the leakage reactance = 3.95 mH. This energy now needs to be dissipated in the snubber.

When the RCD snubber is used as a voltage clamping circuit they are used to clip the voltage spikes that occurs because of the resonance of the leakage inductance with the output capacitance of the reinjection IGBT. IGBTs have a maximum V_{ce} voltage which should not be exceeded. The clamp can be designed so that this maximum voltage is never exceeded. The value of the capacitor can be determined by selecting how much voltage change can occur. The ripple voltage is denoted as dV. The value of capacitor can be determined as:

$$\frac{1}{2}CV^2 + \frac{1}{2}LI^2 = \frac{1}{2}C(V + dV)^2 \tag{C.1}$$

where $\frac{1}{2}CV^2$: is the initial energy stored in the capacitor, $\frac{1}{2}LI^2$: is inductor energy and $\frac{1}{2}C(V + dV)^2$: is the fully charged capacitor. On solving (C.1), the snubber value is:

$$C = \frac{LI^2}{dV(dV + 2V)} \tag{C.2}$$

From calculations - maximum voltage appearing across IGBT = 36.72 V, maximum IGBT current = 1 A, calculated leakage inductance L_{lk} = 3.95 mH, assumed ripple voltage = 40 V, the snubber capacitance = 0.87 μF. Resistance is chosen to be less than 166.66 μs ($\frac{1}{10}^{th}$ of switching time of S_{p0}/S_{n0} reinjection IGBT pair). Hence, $\tau_{RC} = 50$ μs, where snubber resistance = 57Ω/2W.

Considering the leakage reactance, a much higher snubber capacitance is needed than what was used by the trial and error method with McMurray's equation. But when snubber capacitance = 1 μF is used, improvement in voltage waveforms was evident while the current waveforms were highly distorted. A different snubber capacitor value to the one calculated using McMurrays equation improved the voltage waveform. This was due to a different mechanism causing the voltage spike (as elaborated on in the next section) than the typical inductive energy in the transformer leakage reactance having to be controlled by the snubber circuit at turn-off.

C.2 DEAD TIME IN THE REINJECTION CIRCUIT

Initially, there was no dead time implemented in the experimental setup. However, on powering up the MLCR CSC circuit, there was a short circuit which was observed with blown IGBT switches. After inspection it was decided to have a small dead time between the reinjection

circuit to alleviate the problem. However, getting a fixed dead time was a problem with analog components because of component tolerance variations, hence a dead time of 10μs was decided upon. This value was chosen as it encompassed all the variation in the switching pulse edges for the reinjection switches.

However, implementing dead time caused voltage spikes. Each time S_{p0}/S_{n0} (in PSCAD/EMTDC simulation, the switches overlap and no dead time is implemented) is opened, I_{dc} is interrupted, causing a voltage spike across load inductance L_{dc}. From Fig. 6.17, it can be seen that there is variation in the sizes of the spikes, yet they repeat in a pattern. This can be attributed to the variation in the dead-time due to component tolerances. Hence, the inductive energy in the load is a major contributor to the voltage spikes. Digital implementation of entire control circuit should improve the problem of voltage spikes. The issue of enabling the overlapping of switching waveforms without destroying the IGBTs to improve the voltage waveform is an issue which needs to be addressed in future. Another way of controlling the voltage spikes would be the addition of a freewheeling diode to carry I_{dc} when all the reinjection switches are open or implementing a clamp circuit across the load.

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